RACAL
INSTRUMENTS

9916
UHF Frequency Meter
Workshop Manual

Courtesy of:-

Ron G7DOE
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Repair and Restoration
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Robin T. Greenwood
2 | 2002.

WORKSHOP MANUAL

RACAL

Frequency Counter

Model

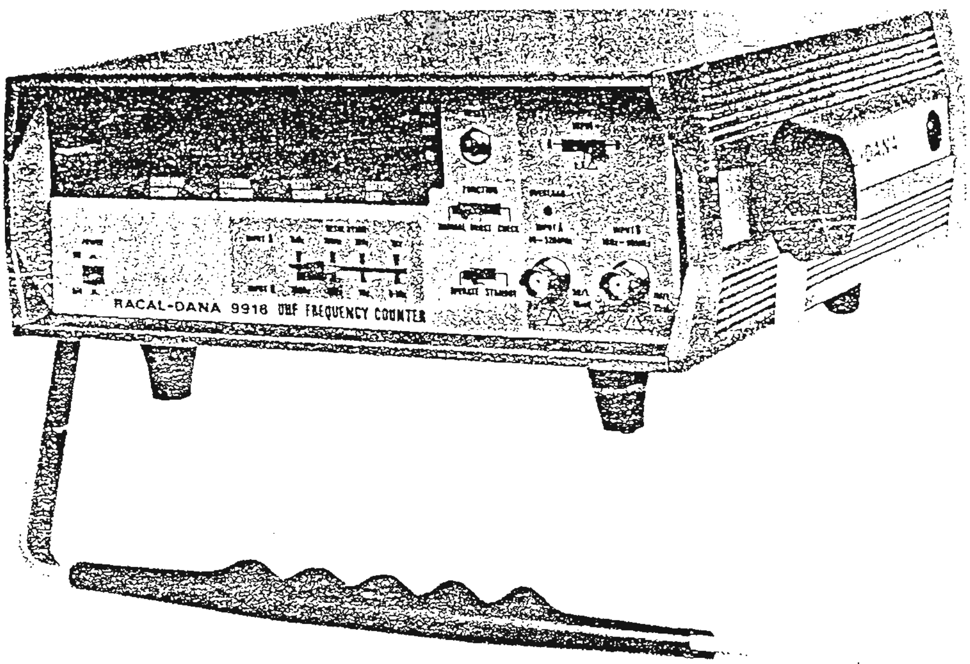
9916

RS Part No 817-117 5v 500Ω coil

Overload Relay RLA available from

Pickering Electronics
Stephenson Road
Clacton-on-sea
Essex CO15 4NL

Tel 01255-428141



UHF Frequency Counter 9916

RACAL

WOH 8153

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

'POZIDRIV' SCREWDRIVERS

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SECTION 1

TECHNICAL SPECIFICATION

TECHNICAL SPECIFICATION

1. DISPLAY

Format:	Eight digit in-line, 7 segment l.e.d. display plus overflow indicator. Decimal point positioned automatically.
Latch:	Previous measurement is displayed during the period required to complete a new measurement. The display is updated automatically at the end of each measurement.
Display Time:	Approximately equal to gate time plus 1 ms.
Reset:	A push button Reset switch resets the reading to zero when pressed and released.
Check:	With the Function switch in the CHECK position the display shows: Channel 'A' - All digits set to 8 to check all segments. Channel 'B' - Counter reads 1 MHz to check operation.
Gate/Charging Indicator:	Lights when the gate is open or batteries are being charged at the full rate.
Battery Low Indicator:	Lights when batteries are low.
Overload Indicator:	Lights when 'A' channel input exceeds about 5V r.m.s.
Overflow/Standby Indicator:	Lights when display is 'overfilled' or when on Standby mode.
External Standard Indicator:	Lights when external frequency standard is connected and switched on.
Display Units Indicators:	Light to indicate the units in which the display should be read.

2. INPUT 'A'

Frequency Range:	40 MHz to 520 MHz.
Sensitivity:	Better than 10 mV.
Signal Range:	10 mV to 5V r.m.s. with automatic gain control.
Input Impedance:	50Ω nominal.
Overload Protection:	Up to 35V r.m.s. maximum by p.i.n. diode attenuator and reed relay.
Prescaling:	Input frequencies are prescaled by a factor of ten.
Automatic Gain Control:	50 dB minimum range. AGC output is available at two pins on rear panel.

3. INPUT 'B'

Frequency Range:	10 Hz to 60 MHz.
Sensitivity:	Better than 10 mV.
Automatic Gain Control:	Approximately 50 dB range.
Input Impedance:	1 MΩ in parallel with approximately 25 pF.
Maximum Signal Levels:	250V r.m.s. up to 10 kHz. 50V r.m.s. up to 100 kHz. 10V r.m.s. above 100 kHz.
Maximum Input Level:	The d.c. level + peak signal level must not exceed 400V over the full frequency range.

4. FREQUENCY MEASUREMENT

Range:	Channel 'A' 40 MHz to 520 MHz (prescaled by 10). Channel 'B' 10 Hz to 60 MHz (direct).
Accuracy:	± 1 count ± frequency standard accuracy.
Gate Times:	0.01s, 0.1s, 1.0s, 10s.

FREQUENCY MEASUREMENT (Cont'd.)

Resolution:	Channel 'A': 1 kHz, 100 Hz, 10 Hz, 1 Hz. Channel 'B': 100 Hz, 10 Hz, 1 Hz, 0.1 Hz.
Burst Mode:	In the Burst Mode the gate remains closed until triggered by incoming signal. After measurement the display is held until manually reset. The minimum signal duration is 40 ms plus gate time.
L.F. Multiplier Facility:	See Option 09.

5. FREQUENCY STANDARD

Internal Frequency Standard:	Refer to Options 04A, 04B and 04C on page Tech. Spec. (5).

6. FREQUENCY STANDARD OUTPUT

Frequency:	1 MHz.
Level:	Standard t.t.l. output giving approximately 600 mV peak to peak into 50Ω.
Output Impedance:	Approximately 200Ω.
Waveform:	Rectangular.

7. EXTERNAL STANDARD INPUT

Frequency:	1 MHz.
Minimum Signal Level:	100 mV r.m.s.
Maximum Signal Level:	10V r.m.s.
Maximum Input Level:	The d.c. level + peak signal level must not exceed 400V.
Input Impedance:	Approximately 200 ohms (a.c. coupled).

8. DATA OUTPUTS

Display, Function and Control:	Serial BCD output is provided at standard t.t.l. logic levels giving 8 digits and decimal point. Static timebase and overflow outputs with timing controls are provided.

9. POWER REQUIREMENTS

AC Supply: 94V to 132V and 188V to 265V r.m.s., 45 to 450 Hz.

Voltage Ranges (a.c.): Six pairs of ranges selected by transformer connections and a link. A rear panel switch selects between the upper and lower range of each pair.

(1) 94-106V/106-119V

(2) 106-119V/118-132V

(3) 188-212V/200-225V

(4) 200-225V/212-238V

(5) 212-238V/224-251V

(6) 224-251V/235-265V

Refer to Chapter 5 for setting instructions.

Consumption: 19 VA approximately.

10. ENVIRONMENTAL AND SAFETY SPECIFICATIONS

Operating Temperature: 0° to $+55^\circ C$ ($0^\circ C$ to $+40^\circ C$ with Battery Option).

Storage Temperature: $-40^\circ C$ to $+70^\circ C$ ($0^\circ C$ to $+60^\circ C$ with Battery Option).

Humidity: 95% r.h. at $+40^\circ C$

Mechanical: In accordance with IEC 68.

Safety: Meets IEC 348 (BS 4743)

11. MECHANICAL

Dimensions:

Height:	110 mm
Width:	284 mm
Depth:	268 mm

Weight: Approximately 2.7 Kg excluding Battery Pack. Battery Pack 1.5 Kg.

12. OPTION 01 SERIAL TO PARALLEL INTERFACE

Purpose: This unit provides an interface between the 28-way data output of the 9916 and a 50-way connector to a printer, or remote display. It converts the serial b.c.d. data to parallel format and transfers the following information: 8 decades of data in 4 line BCD weighted 1248, 3 line decimal point position, print command, print hold, reset, overflow and time-base information. All logic levels are t.t.l. compatible.

13. OPTION 04A: FREQUENCY STANDARD 9442

Type:	A fast warm-up ovened oscillator suitable for the majority of applications.
Frequency:	5 MHz.
Ageing Rate:	± 3 parts in 10^9/ day averaged over a minimum of 10 days after 3 months continuous operation.
Warm-up Time:	Better than ± 2 parts in 10^7 within 6 minutes.
Temperature Stability:	Better than ± 3 parts in 10^9 per $^{\circ}$C averaged over the range -10°C to +45°C, but operable to +55°C.

14. OPTION 04B FREQUENCY STANDARD 9421

Type:	An ovened oscillator of the utmost precision for use when the highest long term accuracy is essential.	
Ageing Rate:	Initial:	± 2 parts in 10^9 per day averaged over a minimum of 10 days at shipment.
	Long Term:	± 5 parts in 10^{10}/ day averaged over a minimum of 10 days after 3 months continuous operation.
Warm-up Time:	Better than ± 1 part in 10^7 within 20 minutes.	
Temperature Stability:	Better than ± 6 parts in 10^{10} per $^{\circ}$C averaged over the range -10°C to +45°C, but operable to +55°C.	

15. OPTION 04C: FREQUENCY STANDARD 11-1254

Type:	An unovened crystal oscillator suitable for non-critical applications or where the instrument will normally be used with the customer's external standard.
Frequency:	5 MHz.
Ageing Rate:	± 1 part in 10^6 per month three months after delivery, but less than ± 1 part in 10^5 in the first year.
Temperature:	± 8 parts in 10^6 over temperature range 0°C to $+55^\circ$C. ± 3 parts in 10^6 over temperature range $+20^\circ$C to $+40^\circ$C.

16. BATTERY POWER PACK OPTION: PART No. 11-1289

Mechanical:	Battery Pack is mounted on a metal tray inside the instrument and connected via a polarised 4 pin connector.
Selection:	By means of 3 position LINE POWER/CHARGE/ BATTERY POWER switch on rear panel.
Battery Life:	4½ hours minimum continuous at $+20^\circ$C. 15 hours minimum on standby at $+20^\circ$C.
Battery Condition:	Indicated by 'Battery Low' lamp on front panel.
Charge Time:	14 hours at $+20^\circ$C.
Standby Facility:	With STANDBY selected, only the internal standard is operational. Pressing the Reset button activates the counter for approximately 1 minute after which it reverts to the standby condition.

17. OPTION 09 FREQUENCY MULTIPLIER

Function:	To increase measurement resolution at low frequencies on 'B' input channel.
Frequency Range:	10 Hz to 25 k Hz.
Multiplication:	x 100
Resolution:	As selected by Resolution switch.

18. OPTIONAL ACCESSORIES

Accessories available:	Rigid carrying case (15-0450) Padded carrying case (15-0444) 19 inch rack mounting kit (11-1126) Data output connector (23-5147)

SUPPLEMENTARY DATA

DATA OUTPUT CONNECTIONS

A1. Data and Command information is available via a 28-way edge connector accessible by removing a cover on the rear panel. The facilities and pin connections are listed in Table 1.

TABLE 1

Data Output Connector

Pin	Facility	Pin	Facility
1	-5V nominal	A	0V
2	+5V nominal	B	$\overline{\text{Overflow}}$
3	Key Way	C	Key Way
4	$\overline{4}$ (BCD)	D	$\overline{1}$ (BCD)
5	$\overline{8}$ (BCD)	E	$\overline{2}$ (BCD)
6	$\overline{\text{External Hold Input}}$	F	10 kHz Sync.
7	$\overline{\text{External Reset Input}}$	H	$\overline{\text{Main Gate}}$
8	Not Used	J	Not Used
9	$\overline{c}$)	K	$\overline{z}$) Time Base
10	$\overline{b}$) Logic '1'	L	$\overline{y}$) Information
11	$\overline{a}$)	M	$\overline{x}$) (See Table 2)
12	$\overline{\text{R (o)}}$	N	Not Used
13	$\overline{\text{Hold/Reset}}$	P	Not Used
14	$\overline{\text{Prescale}}$	R	Not Used

NOTES 1: All facilities are outputs except pins 6 and 7.

2: The Overflow level on pin B is a static indication.

3: The Prescale information on pin 14 is a permanent '1' level to indicate that no correction is required externally to the outputs as the decimal point information is automatically corrected on change of function and channel.

TIME BASE CONTROL LOGIC

A2. The function and time base requirements are applied internally to the CDI chip on six-lines. The inverse states of this code are fed out to the rear Data Output connector. As the 9916 is a single function instrument the $\overline{a}$, $\overline{b}$, $\overline{c}$ 'function' lines are held permanently at logic '1'. The time base information code is given in Table 2.

TABLE 2

Time Base Selection Code

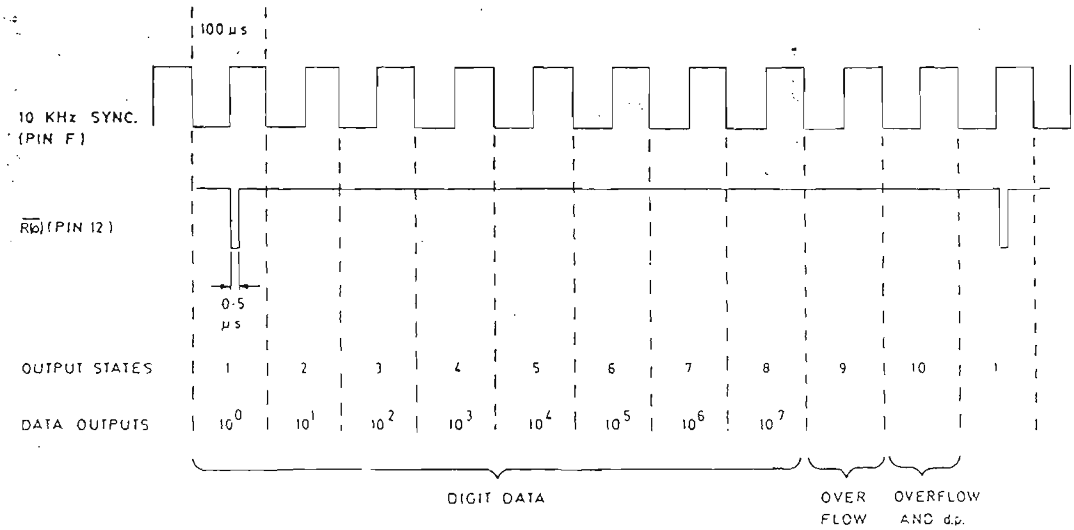
Code			Gate Time	Resolution	
$\overline{x}$	$\overline{y}$	$\overline{z}$		Channel A	Channel B
PINS 8	7	10			
0	1	1	10 ms	1 kHz	100 Hz
1	0	1	100 ms	100 Hz	10 Hz
0	0	1	1 s	10 Hz	1 Hz
1	1	0	10s	1 Hz	0.1 Hz

DATA OUTPUT FORMAT

A3. The b.c.d. output data is available at the 28-way edge connector in a bit parallel, byte serial form. The data is sequenced by a 10 kHz synchronising signal. The data presentation is delayed 0.5 µs from the negative edge of the synchronising signal. An additional synchronising pulse R(o) determines the first state (10^0 digit). Figure A1 (not drawn to scale) shows the timing sequence for the ten states.

A4. The ten data output states are as follows:-

States	Facility
1 to 8	Digit (display) information.
9	Overflow for 10^3, 10^4, 10^6 and 10^7 digits on pins D, E, 4 and 5 respectively.
10	Decimal point position in kHz units, plus overflow information for 10^5 digit (relative to directly gated input) via pin 5.



Data Sequence Diagram Fig A.1

SECTION 2

DESCRIPTION

OPERATION & MAINTENANCE

CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1.1 The 9916 is an eight digit frequency counter with a measurement capability of over 520 MHz and containing a number of advanced operational features. The instrument operates from a.c. supplies or an optional internal battery pack. Built in battery charging façilities are provided.

1.2 Four gate times of .01, 0.1, 1 and 10 seconds are provided. The switch positions are marked with the resolution of the display. A GATE/CHARGING lamp lights when measurement is in progress. An OVERFLOW/STANDBY lamp lights when the display is over-filled or when the instrument is in the Standby mode. The display and all indicator lamps are l.e.d.'s (light-emitting diodes).

INPUTS

1.3 Two input channels are provided. Input 'B' is a directly gated, high impedance channel for frequencies up to 60 MHz with a.g.c. Input 'A' is a 50 ohm channel covering the range 40 MHz to 520 MHz, prescaled by ten and with a.g.c., automatic overload protection and l.e.d. overload indicator.

SPECIAL FEATURES

Large Scale Integration

1.4 The heart of the instrument is an integrated circuit element IC4 which performs all the measuring functions of an 8-digit 60 MHz counter.

'Burst' Measurement

1.5 This facility is provided for measurements on signals which occur in short bursts at irregular intervals. The minimum burst duration for the 'A' and 'B' input channels is 40 ms plus the gate time.

Battery Economy (Standby) Facility

1.6 When the optional battery pack is fitted and continuous readout is not required, a significant increase in battery operating time can be obtained by switching to STANDBY. The instrument is then 'off' except for the internal frequency standard. If the RESET button is depressed the instrument will operate normally for approximately one minute, after which it reverts to the standby conditions. This operation may be repeated as required.

Low Frequency Multiplier (Option)

1.7 An optional 'LF' facility is available for measurement of low frequencies such as audio tones. By means of a frequency multiplication technique the resolution below 25 kHz is improved by a factor of 100. The Burst facility is not operative in the LF mode. If the LF mode is selected when the option is not fitted the display will show all eights.

AGC Output

1.8 The 'A' Channel amplifier a.g.c. voltage is brought out to two pins on the rear panel (AGC O/P) for use as a peak indication, in, for example, transmitter tuning.

Check Facilities

1.9 By selecting INPUT 'A' and CHECK, the readout will display 'all 8's', thus checking that the segments in the numerical indicators are functioning correctly. When LF or Input 'B' and CHECK are selected an internal standard frequency is measured to provide a check of the counting and display circuits.

FREQUENCY STANDARD

1.10 At the customer's option one of three 5 MHz oscillators from the Racal-Dana range can be fitted. Details will be found in the Technical Specification. Option 04C is a discrete component oscillator, and a parts list and circuit will be found in Section 3 of his manual. Options 04A and 04B should be serviced only by Racal-Dana Instruments Ltd., r their agents. For all options an aperture in the rear panel provides access for calibration.

.11 An external frequency standard, which will automatically override the internal standard, can be applied via a BNC socket on the rear panel. A l.e.d. dicator lights when the instrument is operating on the external standard.

A. (Line Power) SUPPLY

1.12 The instrument operates from a.c. supplies between 94V and 132V and between 188V and 265V, 45 to 450 Hz. Tappings and a link on the internal line t nsformer provide a choice of six voltage ranges. A rear panel switch must be set to select either the upper or lower half of the chosen range. Detailed instructions are given in Chapter 5. It is important that the label on the rear panel indicates the selected range.

BATTERY POWER SUPPLY (OPTION)

1.13 The batteries allow $4\frac{1}{2}$ hours continuous operation from the fully charged condition. A 3-position rear panel switch selects ac line power or battery power, or full rate charging of the batteries from the internal charging circuit. When on battery operation a warning light indicates when battery voltage is low. To fully charge a discharged battery requires 14 hours. Avoid overcharging as it will progressively reduce battery charge capacity. When the instrument is operating from a.c. supplies the batteries receive a trickle charge which can continue indefinitely without detriment to the batteries.

CHAPTER 2

OPERATING INSTRUCTIONS

POWER SUPPLY

2.1 AC Supply: Before operating a new instrument, or at a new location, check that the voltage selection is correct (see rear panel label). Set the rear panel switch to LINE POWER and the POWER switch to ON.

Battery Supply: Set the rear panel switch to BATTERY POWER. Set the POWER switch to ON and verify that the BATTERY LOW indicator does not light.

FREQUENCY MEASUREMENT (NORMAL)

2.2 (1) Set the controls as follows:-

(a) NORMAL/BURST/CHECK switch to NORMAL.
(b) OPERATE/STANDBY switch to OPERATE.
(c) INPUT switch to channel 'A' or 'B' as required.

(2) Connect the external signal to the appropriate input socket 'A' or 'B'. The damage overload input levels are:-

Input 'A'	Input 'B'
35V r.m.s. (overload protection above 5V r.m.s.)	250V r.m.s. up to 10 kHz 50V r.m.s. up to 100 kHz 10V r.m.s. above 100 kHz

(3) Check that the GATE lamp lights.

(4) When using Channel 'A' observe the OVERLOAD indicator. Illumination indicates that the input signal has exceeded 5V r.m.s., that input protection has come into operation and the input impedance will have risen above 50Ω

(5) Set the RESOLUTION switch to fill the display, or as required. Read the display in the units indicated by the units indicators. If required, use the overflow procedure (see next paragraph).

Overflow Procedure

2.3 Enhanced resolution at higher frequencies can be obtained by "overspilling" one or more of the left-hand digits. First, select a short gate time and record the most significant digits displayed. Then select a longer gate time to display the less significant digits to the required resolution. The OVERFLOW indicator will light to show that one or more digits are being overspilled at the longer gate time.

FREQUENCY MEASUREMENT (BURST)

2.4 NOTES 1: The minimum burst duration is 40 ms plus gate time.

2: The user may, if desired, use the BURST mode to obtain a single shot reading from a continuous input signal.

(1) Set the NORMAL/BURST/CHECK switch to BURST. Select the required input channel, and connect signal line to appropriate input socket.

(2) Press and release the RESET button. The display (except the d.p.) will go blank. When a signal burst is received it will be measured and the display held until the RESET button is operated again.

FREQUENCY MEASUREMENT (LF OPTION)

2.5 (1) Set the Channel Selection switch to LF.

(2) Connect the external signal to the 'B' input socket (high impedance). The facility is suitable for signal frequency up to 25 kHz, but not with BURST mode.

(3) Set the RESOLUTION switch as required.

NOTE: When no input signal is applied it is normal for the instrument to show a few counts.

BATTERY ECONOMY OPERATION

2.6 (1) Prepare the instrument for battery power operation (para. 2.1).

(2) Set the OPERATE/STANDBY switch to STANDBY and press and release the RESET button. The instrument will operate for approximately one minute and then revert to standby. To repeat the operation press RESET when required.

(3) The OVERFLOW/STANDBY l.e.d. will light when the instrument is in the standby condition.

STANDBY OPERATION

2.7 The operation described in sub-section 2.6 (2) can be used with the instrument operating on line power. It may be noted that, when switching from OPERATE to STANDBY within one minute of first switching on, the display generally remains on for about a minute before settling into the 'display off' standby condition.

BATTERY CHARGING

2.8 (1) Connect the a.c. supply.

(2) Set the rear panel switch to the CHARGE position.

(3) Set the front panel Power switch to ON. Verify that the CHARGE indicator lights. The time required for a complete re-charge is 14 hours.

NOTE: The batteries receive a trickle charge when the instrument is operated with rear panel switch in the LINE POWER position.

CARRYING HANDLE

2.9 The instrument is fitted with a combined carrying handle and bench stand. To adjust the stand, press in the two handle bosses simultaneously, while setting the stand to the desired position.

DESCRIPTION OF CONTROLS

POWER ON/OFF Switch:

NOTE: The switch function is related to the setting of the rear panel LINE POWER/CHARGE BATTERY POWER switch.

Power ON Position

The instrument will operate from either line power or optional battery supply as selected by the rear panel LINE POWER/CHARGE/BATTERY POWER switch. When CHARGE is selected the Power ON position will give full-rate battery charging.

Power OFF

In the OFF position the charging and operating facilities are switched off, irrepective of the type of power supply.

RESOLUTION Switch:

This four position switch selects the appropriate gate time from the time base to give the required resolution. Generally, the switch will be set so that the measurement just fills the display. The display units are shown by the Units Indicators.

OPERATE/STANDBY Switch:

OPERATE is the normal signal measurement mode.

STANDBY permits use of Battery Economy operation or Standby operation (see paragraphs 2.6 and 2.7) according to the setting of the LINE POWER/CHARGE/BATTERY POWER switch. The internal frequency standard remains powered when STANDBY is selected.

FUNCTION Switch:

NORMAL provides continuous measurement with automatic updating of the display.

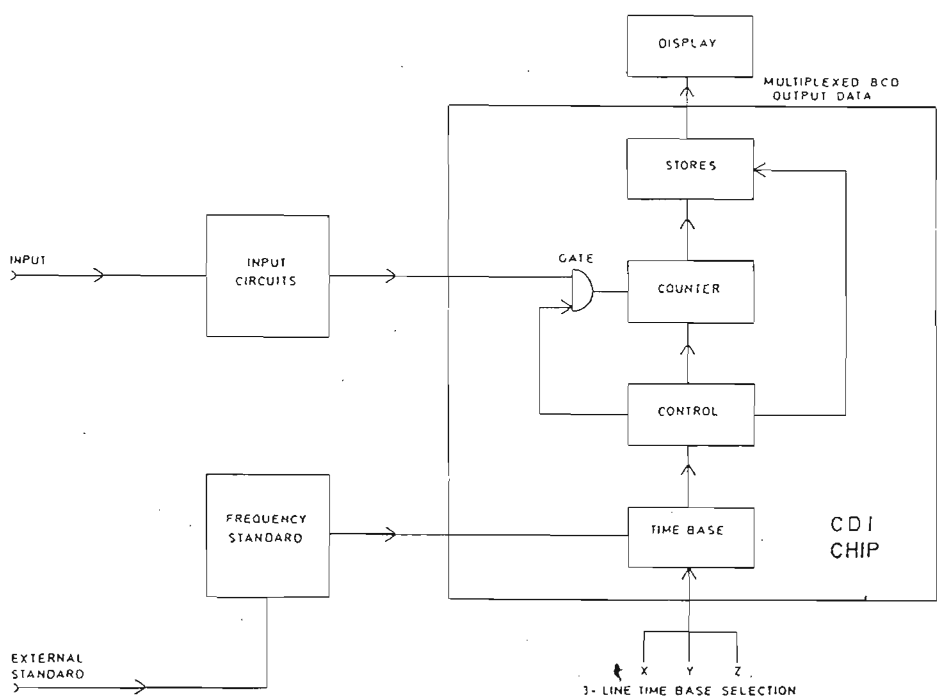
BURST provides a single shot reading from either an intermittent or continuous signal.

CHAPTER 3

PRINCIPLES OF OPERATION

THE CDI CHIP

3.1 A basic digital frequency meter comprises a chain of decade counters feeding b.c.d. data into latched stores. Counting is controlled via a main gate which is opened for a period determined by the time base. Provision is made for resetting the counter and releasing the data for display. In the 9916 these functions are carried out in the integrated circuit IC4, which achieves large scale integration, using the collector-diffusion-isolation principle. For convenience, IC4 will often be referred to in the handbook as the 'CDI Chip'. Fig 3.1 is a simplified diagram of the frequency measurement mode, showing the principal functions performed by the CDI Chip.



Basic Frequency Meter Fig. 3.1

GENERAL CIRCUIT FUNCTIONS

3.2 Outside the CDI Chip, other circuit functions are carried out, as follows:-

(a) Input amplification and signal shaping. AGC and overload protection. Input (channel) selection.

(b) An eight-digit display system in bit-parallel byte serial (multiplex) form, with data readout available for external use.

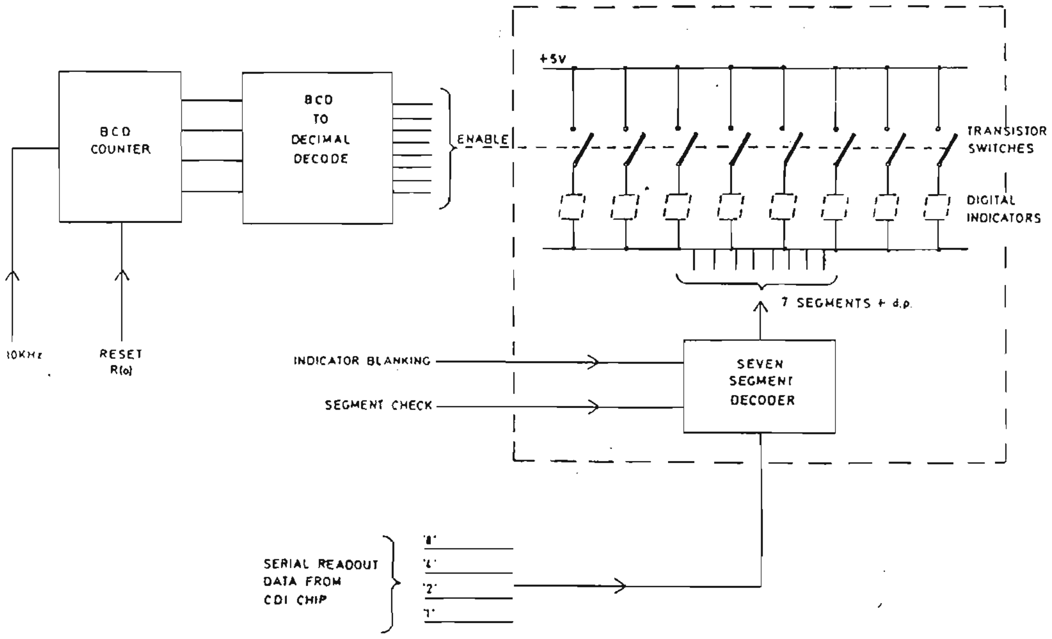
(c) Clock (reference) frequency generation using a discrete 5 MHz oscillator circuit, or a high-stability temperature controlled oscillator. The reference frequency is doubled to 10 MHz for use in the CDI Chip.

(d) The power supply system operates from either a.c. line power or an optional battery pack using re-chargeable nickel-cadmium cells. Trickle charge and full charge facilities are included. 'Charge' and 'Battery Low' indicators are provided. Supplementary power supply circuits provide +24V for the 'A' amplifier and +2V for the CDI Chip. A 'battery economy' facility is provided.

(e) The BURST facility employs circuits which put the counter into the Hold condition with blanked out display. The incoming signal then automatically resets the counter and allows a single measurement to be made and held.

DYNAMIC DISPLAY SYSTEM

3.3 The Display Assembly contains an eight-digit display using light-emitting diodes as numerical indicators. These indicators are driven by b.c.d. data from the CDI Chip, via a seven-segment decoder. Each displayed numeral is formed by lighting an appropriate number of short straight segments. The numeral '8', for example, is formed from 7 segments, whereas the numeral '4' will require only 4 segments.



Multiplex Display System — Fig. 3.2

Multiplex Readout

3.4 The readout data is fed from the CDI Chip to the Display Assembly via a four-line b.c.d. connection. To permit this simple interconnection a parallel-to-serial (multiplex) system is used. The principles are shown in Figure 3.2, although it should be noted that part of the system is in the CDI Chip.

3.5 In the CDI Chip the data stores feed in parallel into a common b.c.d. four-line output. The store outputs are enabled in turn for approximately 100 micro-seconds by a 10 kHz reference signal, derived from the frequency standard.

3.6 The b.c.d. data is fed to a 7-segment decoder (IC1) in the Display Assembly, which offers the decoded data to the bank of l.e.d. numerical indicators. The 10 kHz reference signal is fed to a counter and BCD/Decimal decoder, enabling each indicator in turn for 100 microseconds. A reset pulse R(o) which is generated in the 10^{o} state of the counter ensures that the display enable is synchronised with the data store readout. Provision is made via IC1 for a segment check and also for blanking out the display in BURST mode.

Decimal Point

3.7 Decimal point (d.p.) illumination is obtained by encoding the time base control (RESOLUTION) switch logic with the digital indicator 'enable' signals. The encoder output turns on a d.p. drive transistor at the correct time to light the appropriate decimal point.

CONTROL INFORMATION

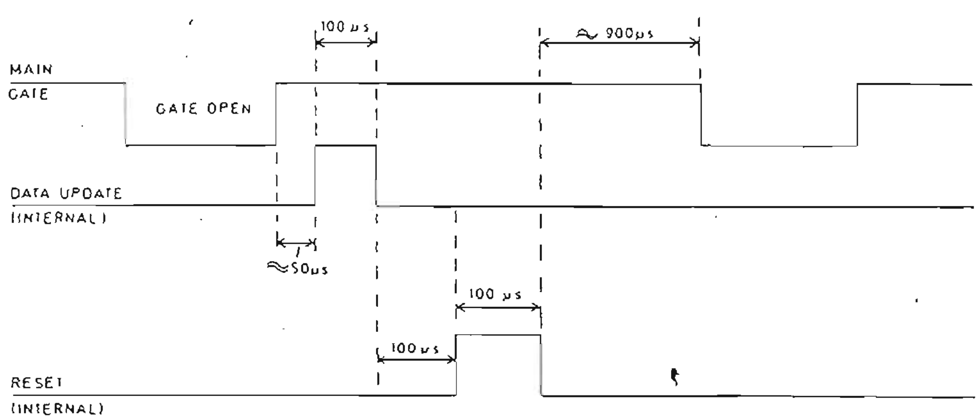
3.8 A 3-line system is used for time base (gate time) selection. The lines are identified as x, y and z, and the logic coding is in Table 2 in the Technical Specification.

RESISTOR ARRAYS

3.9 Many of the integrated circuits are 'open collector' types. For these IC's discrete 'pull-up' resistors are provided in the circuit. These resistors may be mounted in sealed dual-in-line (d.i.l.) packages, for example R108 (Fig. 5) which has thirteen 1k resistors with a common connection to +5V. Such arrays cannot be serviced and must be changed in the event of a faulty resistor. Another type of resistor array comprises a d.i.l. package containing separate resistors of identical values, for example R107 which contains eight 220 ohms resistors.

CONTROL SEQUENCE

3.10 Fig. 3.3 shows the control sequence diagrammatically (not to scale).



Control Sequence Diagram Fig.3·3

External Hold

3.11 If, when used with external circuitry, it is required to extend the cycle time, the external hold, (logic '0', pin 6) must be applied within the gate time or up to 100 μs after gate closure. To initiate a new cycle of measurement, the external hold must go 'high' for not less than 200 μs.

External Reset

3.12 External reset is achieved by the application of logic '0' to pin 7 of the Data Output connector for a period of not less than 100 ns. On returning to '1' level the display resets to 'all zeros' and a new measurement cycle commences.

CHAPTER 4

TECHNICAL DESCRIPTION

INTRODUCTION

4.1 Apart from some switches and certain items of the power supply the circuit for the instrument is mounted on one main p.c.b. assembly, with smaller assemblies for the display, the frequency standard, and the LF Multiplier and Battery Power Supply options.

LOGIC CIRCUIT SYMBOLS

4.2 Extensive use is made of integrated circuits (IC's). These are identified by a number and suffix letter. In the circuit description a particular IC pin will be identified by a reference such as 'IC1a/2', which indicates pin 2 on that particular gate. The logic sysmbols used in the circuits are those found in most manufacturers IC data sheets, to which reference should be made if detailed information is required. The CDI chip IC4 is, however, obtainable only through the Service Department of Racal-Dana Instruments Ltd.

NORMAL MODE

Signal Input

4.3 Two input channels, designated 'A' and 'B', cover the full frequency range of the instrument. Separate input sockets are provided. Details of the frequency coverage are given in the Technical Specification.

'A' Channel Amplifier

4.4 The signal to be measured is applied to the front panel BNC socket SK51, and passes via C36 and the contact of the overload relay RLA-1 to the AGC attenuator. This is a PIN diode network, D11, D12, D13, D14 and D15.

4.5 The signal leaving the attenuator is amplified in a wideband VHF amplifier IC26 and a transistor stage Q9. It is then passed via C50 to the prescaling divider IC18. The output at IC18/4 is passed via the emitter follower Q11 and amplifier stage Q12 to IC9b/3, part of the signal selection system described in paragraph 4.17.

AGC and Attenuator

4.6 The amplified signals at IC18/10 are applied via C49 to the AGC detector D16/C53. Increasing amplitude causes the potential at the D16/C53 junction to go less positive.

4.7 The potential at C53 is applied via R63 and IC25b to the base of Q10. An increase of input signal amplitude causes an increase in potential at Q10 emitter.

4.8 The PIN diodes of the attenuator exhibit an impedance which is inversely proportional to the current carried. As the AGC potential increases D14 current increases, and the potential at the D12/D13 junction increases. This reduces the current carried by D12 and D13, which, in turn, increases the potential at the D11/D12 and D13/D15 junctions and increases the current in D11 and D15. The overall effect is an increase in the impedance of the series attenuator arm and a decrease in impedance of the shunt arms.

4.9 The AGC voltage is available at a two pin outlet on the rear panel to provide an indication of relative amplitude for 'A' Channel signals.

Low Level Inhibit

.10 The output of the AGC detector is applied to IC25a/1. This is an operational amplifier connected as a Schmitt trigger. The triggering level is set by adjusting R64. If the input signal level is too low to give stable counting IC25a/12 is at logic '0', and IC9b, part of the signal selection system described in paragraph 4.17, is inhibited.

Overload Protection and Indication

4.11 Signals applied to the 'A' Channel input are passed to the peak to peak detector C35, D9, D10 and C37. Increasing signal amplitude results in the detector output making IC29/2 more negative via the potential divider R39/R40.

4.12 IC29 is a Schmitt trigger which triggers when pin 2 goes more negative than pin 3. This occurs when the input voltage is approximately 5 volts r.m.s., and de-energises RLA to isolate the amplifier from the input. At the same time Q8 is switched on and lights LP1 to give warning that overload has occurred.

,' Channel Amplifier

4.13 The signal to be measured is applied to the front panel BNC socket SK50, and passes, via C100, R200 and the C1/R3 combination, to the high impedance FET first stage Q1. The gate of Q1 is protected by R3, D1 and the gate/channel diode.

4.14 The output at the source of Q1 is passed via the emitter follower Q2 to the AGC attenuator D2/D3. The attenuator output is amplified in IC30, buffered by Q4, and applied to the Schmitt trigger IC21c. The signal from IC21c passes via a line receiver IC21b, which is used as a gate, to Q5 and IC8b. The output of IC21b is also taken to the Low Frequency Multiplier (if fitted) and then to IC9a. The LF Multiplier is described in paragraph 4.71. IC8b and IC9a are part of the signal selection system described in paragraph 4.17.

AGC and Attenuator

4.15 The signal at Q4 emitter is passed via Q3 to the peak to peak detector C13, D5, D4 and C11. As the input signal amplitude increases the potential across C11 increases. This level is applied via the emitter follower to IC31a, which controls the current in D2 and D3. An increase in input signal increases the current in the diodes, reducing their dynamic impedance. The diodes, in conjunction with R10, form a potential divider across the output of Q2, and a reduction in diode dynamic impedance reduces the signal passed to IC30.

Low Level Inhibit

4.16 The output of the AGC detector is fed to the Schmitt trigger IC31b. If the input signal amplitude is too small for stable counting IC31b/7 is at a lower potential than IC31b/6. The resulting output at IC31b/10, applied to IC21a/13, gives a voltage level at IC21a/15 high enough to inhibit the output of IC21b.

Signal Selection System

4.17 The selection of the 'A' Channel, 'B' Channel or LF multiplier signal to be passed to the counter input IC4/22 is made by the Channel Select switch 1S1 and gates IC18a and b and IC9a and b.

4.18 With the 'A' Channel selected IC9b/5 is set to '1' via IC10a. Provided IC9b/4 is also at '1' (see paragraph 4.10) 'A' Channel signals will pass to IC4/22. IC8b is inhibited by a '0' at pin 12, and IC9a is inhibited by a '0' at pins 1 and 2 from IC10b. At the same time the -5 volt supply is connected to the 'A' Channel and disconnected from the 'B' Channel by the Channel Select switch. The +5 volt supply is connected to the 'A' Channel by Q13, turned on by the Channel Select switch via IC10a and IC13c, and disconnected from the 'B' Channel by Q6, turned off via IC13d.

4.19 With the 'B' Channel selected IC8b is enabled by '1's at pin 12 (from R79), pin 9 (from R81) and pin 10. 'B' Channel signals from Q5 will pass to IC4/22. IC9b is inhibited by a '0' at pin 5 from IC10a, and IC9a is inhibited by a '0' at pins 1 and 2 from IC10b. The -5 volt supply is now connected to the 'B' Channel instead of the 'A' Channel, and Q6 and Q13 connect the +5 volt supply to the 'B' Channel and not to the 'A' Channel. The '1' from R79, inverted by IC10a, puts IC14a into the cleared state, cutting off the +24V supply to IC26 (see paragraph 4.59).

4.20 With LF selected IC9a is enabled by a '1' on pins 1 and 2 from IC10b. IC8b is inhibited by a '0' at pin 10 and IC9b is inhibited by a '0' at pin 5 from IC10a. The power supplies remain connected to the 'B' Channel.

4.21 Selection of LF results in a '0' appearing at IC19d/11. If LK1 is in place this is applied to IC1/3 in the Display Assembly, giving an 'all eights' display. This is to provide warning when LF is selected, but the LF Multiplier option is not fitted. When the option is fitted LK1 should be removed.

Frequency Standard

4.22 A 10 MHz standard is required at IC4/5 or a 1 MHz standard at IC4/20. Three internal oscillator options are available. The specifications are to be found in the Technical Specification. Model 9442 and model 9421 are ovened oscillators. They are precision items, and if a fault develops they should be returned to Racal-Dana Instruments Ltd., or an approved agent for servicing. No parts list or circuit information is provided in this manual.

4.23 When oscillator model 9421 is in use a link must be fitted between pins 5 and 6 on the B7G base.

Oscillator Assembly 11-1254

4.24 This is a discrete component crystal controlled oscillator attached to the rear panel of the instrument. The circuit is shown in Fig. 2. Access to the trimming capacitor C4 is via an aperture in the rear panel.

Internal Standard Buffer

4.25 The internal standard signal is buffered by Q29 and IC3e. The frequency is doubled in the circuit consisting of IC5, IC3d, IC3f, R120 and C80.

External Standard Input

4.26 Provision is made for the use of an external 1 MHz standard, which can be fed in on SK53 on the rear panel. This signal is buffered by Q16, and applied to IC4/20 and to the peak to peak detector C67, D21, D20 and C66. The detector output switches on Q17 to light LP5, indicating that the external standard is in use.

4.27 It is a feature of IC4 that it will automatically change to external standard if an external standard frequency is present. For internal standard operation IC4/20 must be at '0'.

Display System

4.28 The contents of the b.c.d. stores within IC4 are fed in order to the output pins 15, 16, 17 and 18. Each store content is read for 100 μs, controlled by a 10 kHz signal derived from the frequency standard. The b.c.d. output is decoded to 7 segment form in IC1 of the Display Assembly, and offered to the seven segment numerical indicators in parallel.

4.29 The 10 kHz control signal from IC4/7 is counted in the b.c.d. counter IC23, the count being decoded to decimal in IC28. In states 0 to 7 of IC23 the numerical indicators are enabled in turn by the transistor switches Q18 to 25. Since the indicator enabling signal and the store readout are controlled by the same 10 kHz signal each indicator shows the contents of one store.

4.30 To ensure that each numerical indicator shows the contents of the correct store a pulse R(o) is produced coincident with the reading of the 10^0 store. This pulse, available at IC4/14 is used to set IC23 to state 0 at the time of the 10^0 store readout.

Resolution and Decimal Point Selection

4.31 The resolution of the instrument is governed by the period of opening of the main gate, whether the direct or prescaled input is being measured and whether or not the LF multiplier is in use.

4.32 The period of opening of the main gate is controlled by the RESOLUTION switch, which controls the logic on the x, y and z lines to IC4. The logic is shown in Table 2 of the Technical Specification. Increasing the gate time by a factor of 10 effectively shifts the whole display to the left by one digit, and the decimal point must be shifted to correspond.

4.33 The use of the 'A' Channel, which is prescaled by 10, requires the movement of the decimal point to the right by one position, while use of the LF multiplier requires a shift to the left of two positions.

4.34 The decimal point occurs in the numerical indicator which is enabled when Q28, the common decimal point driver, is switched on. This occurs when IC24a/3, IC24b/6 and IC24c/8 are at '1' simultaneously. A '1' applied to one gate from the RESOLUTION switch ensures this is not achieved except when the desired display enable line from IC28 goes to '0'.

4.35 The display enable line is selected by the multiplexers IC20 and IC27. IC20 selects the B inputs when LF is selected, and the decimal point appears in the 10^1, 10^2, or 10^3 numerical indicators. When LF is not selected IC20 accepts the output of IC27. When the 'A' Channel is selected IC27/1 is at '0' and the A inputs are chosen. The decimal point therefore appears in the 10^3, 10^4 or 10^5 position for the 'A' Channel and the 10^4, 10^5 or 10^6 positions for the 'B' Channel.

4.36 Decimal point information relative to the information in the stores in IC4 is available in state 9 of IC23 on the b.c.d. output lines. This information is modified to account for the use of prescaling or LF multiplication before it is made available at the Data Output panel. Modification is made in IC16, where information from IC22b, c and d is added to that from IC4.

4.37 During states 0 to 8 of IC23, IC22c/8 and IC22b/6 are at '1'. The outputs at IC22c/10 and IC22b/4 are therefore at '0', and no modification is made to the b.c.d. information from IC4. During state 9 IC27c/10 goes to '1' if the 'A' Channel is selected but otherwise remains at '0'. IC22b/4 goes to '1' if either LF or the 'A' Channel are selected. Thus, for LF, binary 010 (decimal 2) is added, and for 'A' Channel binary 111 (the 2's complement of 1) is added, so adding two to or subtracting 1 from the b.c.d. information.

Units Indicators

4.38 The units in which the display should be read are indicated by LP2, 3 and 4. These are lit according to the encoding of the logic from the RESOLUTION switch and the CHANNEL SELECT switch (LF position) in IC15a, b, c and d.

Overflow

4.39 Overflow of the 10^7 store is indicated by a '1' at IC4/15 during state 8 of IC23. If overflow occurs IC14b/12 is taken to '1'. During state 8 IC22a/2 goes to '0', and at the negative going transition of the 10 kHz signal at IC22a/3, IC14b/8 is clocked to '0'. This lights LP6 to indicate that overflow has occurred.

4.40 IC14b is returned to the cleared state by a '0' at pin 13 at the end of the main gate period.

Gate Indicator

4.41 The main gate waveform is inverted by IC7a. When the main gate is closed IC7a/2 is at '0' and Q31 turned off. With the main gate open the R130/R135 junction can rise and Q31 turns on. LP7 therefore lights in synchronism with the main gate.
A steady illumination during measurement operation indicates that the counter gating is functioning. The indicator also indicates while the batteries are charging

Display Blanking

.42 The display is blanked out briefly at the end of each gate period while the readout system is synchronising. Q27 is turned off by the trailing edge of the main gate pulse (inverted in IC7a and differentiated by C78/R113). The resulting short negative going pulse at IC19c/8 is applied to 1 IC1/4 and blanks the display.

4.43 The display is also blanked out in the event of failure of the 10 kHz synchronising signal. This prevents burn out of the numerical indicator which is enabled when failure occurs. One digit of the b.c.d. output of IC23 is applied to the peak to peak detector C76, D23, D24, C77. The detector output turns on Q26. If change in the b.c.d. digit ceases Q26 will turn off and IC19b will clamp 1IC1/4 to '0'.

Manual Reset

4.44 Closing S50, the MANUAL RESET push button, puts a '0' on IC17a/2. The resulting '1' at IC17a/12, inverted in IC3b is applied to IC17b/4, giving a '1' at IC4/13 and putting the counter into the HOLD state. The '0' from S50 is also applied to IC2a/9. This gives a negative going pulse, of duration determined by R171/C71 at IC2a/12and IC17a/13. This overcomes any contact bounce effects in S50.

4.45 Releasing S50 allows IC4/13 to revert to '0' and a new measurement cycle to start. The '0' to '1' transition at IC3b/4 is applied to IC13a/2, giving a '0' at IC2b/1. This gives a positive going pulse at IC2b/13which is inverted in IC3c to give a negative going pulse at IC4/4. This unlatches and clears the stores ready for the new measurement.

External Hold and Reset

4.46 The application of a '0' at pin 6 of the Data Output socket results in a '1' at IC17b/6 and IC4/13. Provided this is applied in accordance with the conditions in paragraph 3.11 the counter will go into the Hold state at the end of the measurement in progress.

4.47 The application of a '0' at pin 7 of the Data Output socket results in operation of the reset circuit as described in paragraphs 4.44 and 4.45 except that no bounce protection is provided by IC2a.

BURST MODE

Summary of Operation

4.48 With the FUNCTION switch set to BURST the counter is put into the Hold state. Pressing the RESET button extinguishes the display except for the decimal point. The incoming signal to be measured causes the counter to reset and commence a 'one-shot' measurement.. As measurement commences the display shows all zeros. At the end of the measurement period the display is updated and the counter reverts to the Hold state. A fresh cycle is initiated by pressing and releasing the RESET push button.

Circuit Operation

4.49 When BURST is selected the Burst Select line is at '1'. IC17c therefore has all its inputs at '1', provided Q26 is on (see paragraph 4.43). This produces a '0' at IC17b/5 and a '1' at IC4/13, putting the counter into the Hold state.

4.50 When the RESET button is pressed a '0' is applied at IC12b/10 via the reset circuitry. This puts IC12b into the preset state. IC12b/9 goes to '1', which is applied to IC19a/2. Since IC19a/1 is at '1' when BURST is selected IC19a puts a '0' onto 11C1/4, blanking the display. IC12b/8 goes to '0', holding IC12a in the cleared state. When the RESET button is released IC12b is freed from the preset condition, and can respond to clocking signals.

4.51 The incoming signal to be measured is applied to IC12b/11, clocking IC12b/9 to '0' and IC12b/8 to '1'. The '0' is applied to IC19a/2, removing the display blanking. It is also applied to IC12a/2 via C68. When the '1' at IC12b/8 releases IC12a from the cleared state it can be clocked by the 10 kHz signal at IC12a/3, but since IC12a/2 is at '0' no change of state occurs. As C68 charges, however, IC12a/2 reverts to the '1' state, and after a delay of 40 ms IC12a/6 is clocked to '0'. This delay provides settling time for the input amplifiers.

4.52 The step at IC12a/6, differentiated by C69 and R94/R96, is fed to IC17c/9 giving a positive going pulse at IC17b/5 and IC13a/1. IC4/13 is taken to '0' by IC17b for the pulse duration, initiating a new measurement cycle on the '1' to '0' transition and then returning to the Hold condition so that the display will be held at the end of the gate period. IC13a/3 goes to '0' and causes IC2b to generate a stores update pulse at IC4/4. The circuit will remain in this condition until the RESET button is pressed again.

CHECK MODE

4.53 With the FUNCTION switch set to CHECK IC8b/9 is at '0', IC9c/9 and 10 are at '1' and IC24d/13 is at '1'. If 'A' Channel is also selected IC10a/1 is at '0', putting IC24d/12 to '1'. IC24d/11 therefore goes to '0', and this level, applied to 11C1/3 gives an 'all eights' display for segment checking.

4.54 With CHECK and 'B' Channel selected IC8b is inhibited by the '0' at pin 9, IC9a is inhibited by the '0' at pins 1 and 2, IC9b is inhibited by the '0' at pin 5. IC9c is enabled by a '1' on pins 9 and 10, and passes the 1 MHz from IC4/6 to the counter circuits.

POWER SUPPLY

Line Power

4.55 With the LINE POWER/CHARGE/BATTERY POWER switch (S2) at LINE POWER the supply is fed via a 3-pin plug/filter connector on the rear panel, fuse FS50, the POWER switch and S52 to the primaries of T50. The transformer tappings and S52 must be set to suit the local supply voltage as shown in Fig. 5.1.

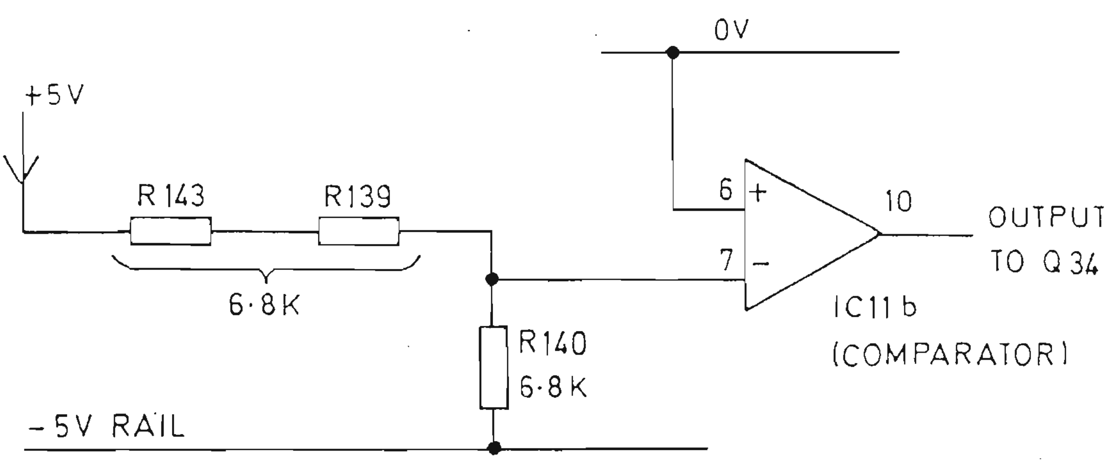
4.56 The output of secondary 'A' is rectified in the potted bridge rectifier D50 and smoothed by C101 to provide a supply for the +5 volt stabiliser. The output of secondary 'B' is rectified in the diode bridge D31 to D34 and smoothed by C102 to provide the -5 volt stabiliser supply. The -5 volt rail is protected by FS1, which must be of the quick action type.

+5 Volt Stabiliser

4.57 When the POWER switch is set to ON D28 is connected between the +5 volt rail and 0 volts. This turns on Q33, which turns on Q36. Q36 draws current through D30 to provide a voltage at IC11a/2. IC11a compares this voltage with 0 volts, and regulates the volt drop across Q51 (via Q32) to maintain a constant potential on the +5 volt rail.

-5 Volt Stabiliser

4.58 The -5 volt rail is stabilised by Q52, which is controlled by IC11b (via Q34). The voltage at IC11b/7, derived from the potentiometer chain R143, R139, R140 is compared with 0 volts at IC11b/6.



-5V Stabilizer Fig. 4.1

-24 Volt Supply

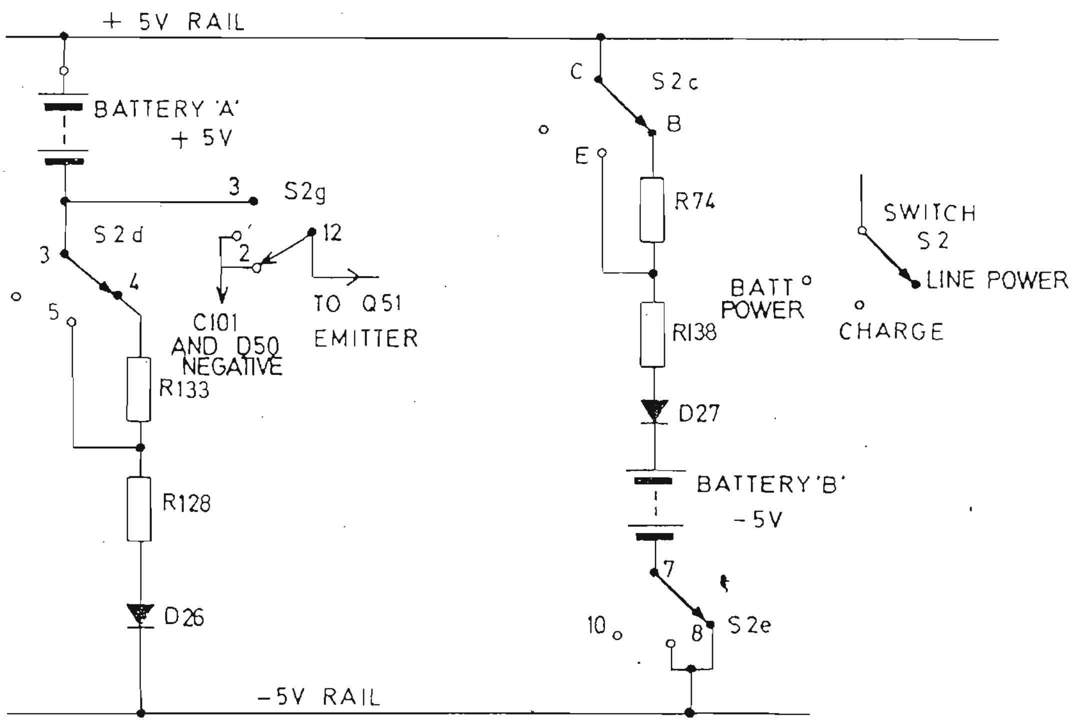
4.59 The 1 MHz signal from IC4/6 is used to clock IC14a. This is connected to divide by two, so that Q7 is driven at 500 kHz. The oscillation in T1 is rectified by D6 and D7, and boosts the +5 volts to +24 volts to supply IC26. The supply is present only when the 'A' Channel is selected as in other conditions IC14a is held in the cleared state.

+2 Volt Supply

4.60 A +2 volt supply is obtained for IC4 from the +5 volt supply via the regulator Q14. Q14 is controlled by Q15, which obtains its reference voltage from IC4/11.

Battery Charging

4.61 If fitted, the batteries receive trickle charge whenever the instrument is operating from a line power supply. Each battery is connected between the +5 volt and -5 volt rails, as shown in Fig. 4.2. The diodes D26 and D27 prevent the batteries discharging if the supply is disconnected with the instrument switched on.



Battery Charging Circuit Fig. 4.2

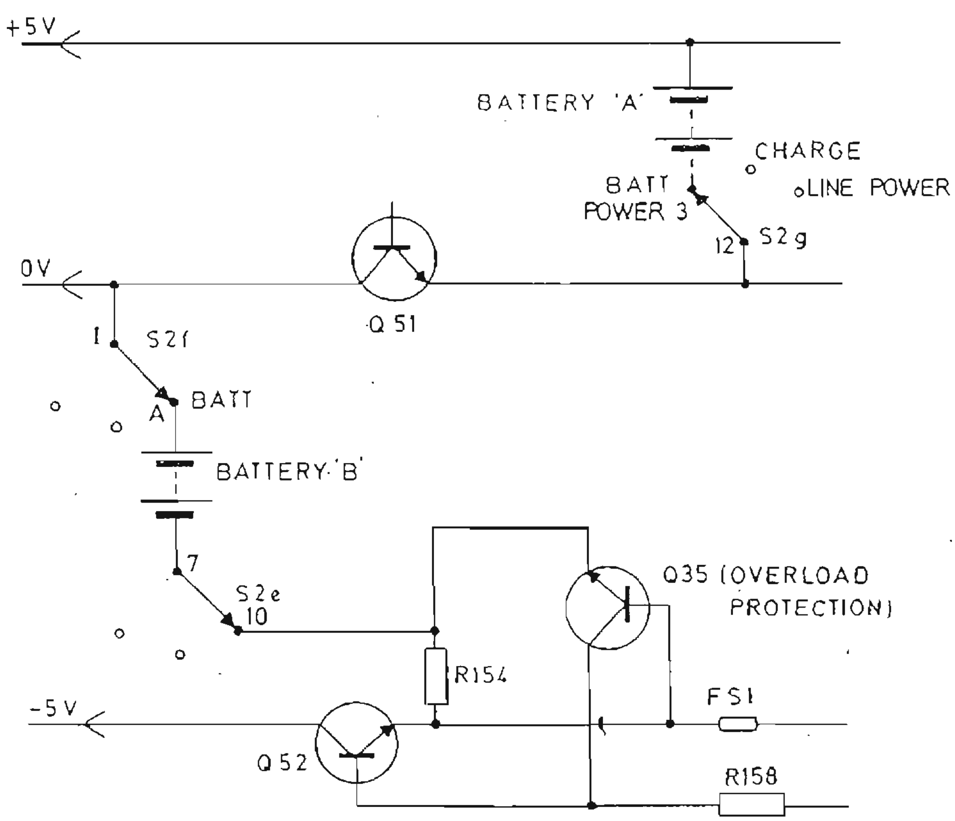
4.62 Putting S2 to the CHARGE position bypasses R133 and R134, which increases the charging rate by approximately 10 times.

Charge Indicator

4.63 The anode of LP7 is supplied from the +5 volt rail at the collector of Q50. The same supply turns on Q31 via R130 and R135 since, when CHARGE is selected, there is no supply to IC7 and therefore no clamping action at the R130/R135 junction.

Battery Power

4.64 With S2 set to BATTERY POWER the batteries are connected as shown in Fig. 4.3.



Battery Power System Fig. 4.3

Battery Low Indicator

4.65 IC6a/1 is connected to 0 volts at Q51 collector. The non-inverting input is connected to the junction of R155/R152, which is approximately 0.5 volt positive with respect to Q51 emitter. When the volt drop across Q51 falls to about 0.5 volt IC6/1 is at a potential below that of IC6/2 and IC6/12 goes to '1', lighting LP8.

Over Discharge Protection

4.66 The Battery Low indicator lights when only a few minutes of battery life remain. If this warning is disregarded the instrument will shut itself off to prevent battery damage.

4.67 R150 and D28 are connected across Battery A. If the voltage falls below about 5 volts Q33 will start to turn off. This will turn off Q36 and render D30 ineffective as the source of reference voltage for IC11a. The voltage of the +5 volt rail will fall and the instrument will cease to draw current.

Overload Protection

4.68 Battery B is protected by Q35. In the event of overload the potential across R154 will turn Q35 on, and so shunt the base current away from Q52. This limits the current available from the -5 volt supply.

STANDBY OPERATION

4.69 With 1S3 at OPERATE the base of Q50 is connected to ground via R125, and it is able to conduct. With the switch at STANDBY Q50 is cut off because Q30 is normally cut off by IC6b. This disconnects the +5 volt rail and removes the reference for the -5 volt regulator. The internal frequency standard remains powered from a connection at Q50 emitter. LP6 anode is also supplied from this point, and since the +5 volt supply rail is at 0 volts is able to light via 1R3 to indicate the Standby condition.

Battery Economy Operation

4.70 Pressing the RESET push button while STANDBY is selected causes rapid discharge of C83 via D25. This results in the potential of IC6b/7 falling below that of IC6b/6, and IC6b/10 goes high, switching on Q30 and therefore Q50. This restores the supplies, and the instrument will operate normally until C83 recharges via R131 and triggers IC6b back to its original condition. This takes about one minute. The OVERFLOW/STANDBY indicator lights when the instrument reverts to the Standby condition.

LF MULTIPLIER 11-1255

Principle

4.71 Frequency multiplication is achieved by a voltage controlled oscillator which is set to run at 100 times the input frequency. The oscillator control is derived from phase comparison of the frequency divided output of the oscillator with the incoming frequency.

Circuit Description (Fig. 6)

4.72 The LF signal is fed to the p.c.b. at pin 2, and passes via C1 to IC1/2. IC1 is an operational amplifier having feedback which gives Schmitt trigger characteristics. An input of 400 mV peak to peak will give an output of approximately 6V peak to peak.

4.73 IC2 contains a voltage controlled oscillator operating in a phase locked loop. The output of IC1 is fed to one of the phase comparator inputs IC2/14. The oscillator frequency is controlled by:

(1) The voltage at IC2/9.

(2) The resistance from IC2/11 to the negative rail.

(3) The capacitance between IC2/6 and IC2/7.

(4) The phase comparator output at IC2/13.

4.74 The oscillator output at IC2/4 is fed via Q3 to a dual decade divider, IC3. From IC3/13 the divided signal is fed back via Q2 to the second phase comparator input IC2/3. The phase comparator output at IC2/13 is fed to the oscillator control connection IC2/9, and results in the oscillator running at a precise multiple of the input frequency.

4.75 The division ratio required in IC3 is 100. This is set by the fitting of link LK2. When fitting a new LF multiplier p.c.b. ensure that LK2 is fitted between pins 3 and 4 of IC3 and that LK1 is not fitted.

CHAPTER 5

MAINTENANCE

TABLE 3: Test Equipment Required

Item	Preferred Item	Remarks
1	Multimeter Danameter 2000A	AC range 0 to 250 volts DC range 0 to 30 volts, 30kΩ/volt Ohms range 150Ω mid scale
2	Oscilloscope BWD 525	Bandwidth d.c. to 50 MHz Y Sensitivity 50 mV/cm.
3	Frequency Standard	1 MHz accurate to ± 1 part in 10^8 Output 1 volt r.m.s. nominal.
4	Signal Generator Racal-Dana 9061/9062/ 9063/9064 combination	Frequency range 8 Hz to 550 MHz Output level from 5mV to 1V r.m.s. into 50Ω The LF signal generator must have a signal to noise ratio better than 40dB.
5	Power Amplifier	To give up to 10 V r.m.s. into 50Ω at 65 MHz.
6	BNC 'T' piece	50Ω
7	BNC Terminating Pad	50Ω
8	Coaxial leads	BNC to BNC connectors, 50Ω 1 metre long, quantity 2 required
9	Variac	To supply 125mA at outputs from 188 volts to 235 volts or 250mA from 94 volts to 118 volts.

REMOVAL OF COVERS

WARNING: DANGEROUS AC VOLTAGES ARE EXPOSED WHEN COVERS ARE REMOVED WITH AC SUPPLY CONNECTED.

5.1 (1) Set the POWER switch to 'off', switch off the a.c. supply at the supply point and unplug the power lead.

(2) Remove four screws from top and bottom covers.

(3) Remove the rubber plugs (located near to the rear end) from both side panels of the instrument and slacken, by about two turns, the screws revealed.

(4) Grip the rear panel assembly and ease it back from the main case to the maximum extent available (about 5 mm).

(5) The rear edge of either cover can now be lifted and the cover withdrawn outwards and rearwards.

(6) To replace the covers reverse the above procedure.

TRANSFORMER VOLTAGE SELECTION

5.2 Ensure the voltage range selected is suitable for the local supply. To check the selection proceed as follows:

(1) Unplug the power cable from the supply and remove the top cover (see paragraph 5.1).

(2) Refer to Fig.5.1 and note the diagram which corresponds to the local supply voltage.

(3) Connect the link and the wires from S52 to the transformer tappings as shown in the appropriate diagram.

(4) Set S52 to the correct half of the selected range.

(5) Ensure that the rear panel label correctly indicates the voltage range selected.

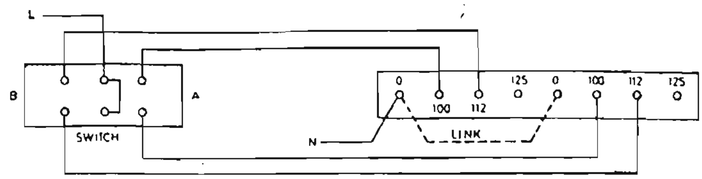
(6) Replace the top cover.

FUSES

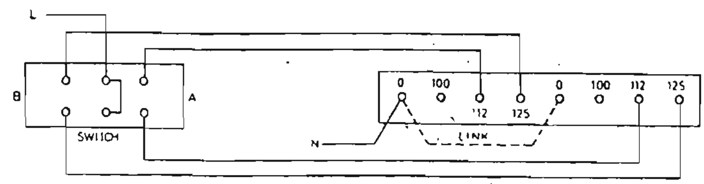
5.3 Check that the power fuse on the rear panel is correctly rated for the supply voltage, as follows. The fuse is a glass cartridge type, 5 x 20 mm.

Supply Range	Fuse Rating	Racal-Dana Part No.
188V to 265V	125mA anti-surge	23-0031
94V to 132	250mA anti-surge	23-0043

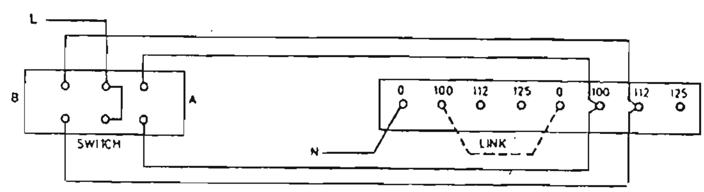
94-106V (SWITCH TO A)
106-119V (SWITCH TO B)



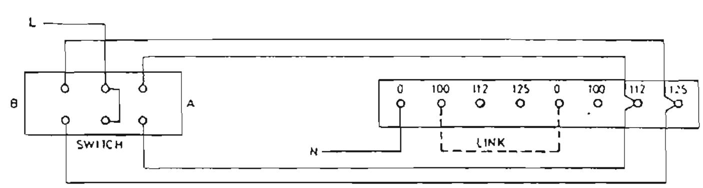
106-119V (SWITCH TO A)
118-132V (SWITCH TO B)



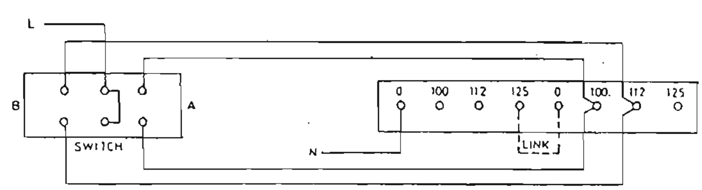
188-212V (SWITCH TO A)
200-225V (SWITCH TO B)



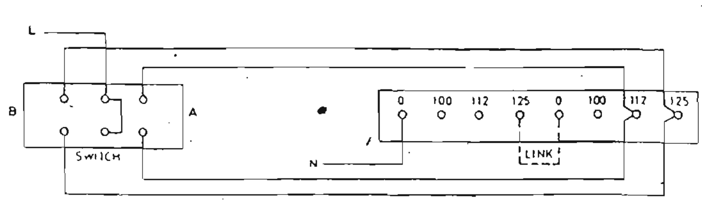
200-225V (SWITCH TO 'A')
212-238V (SWITCH TO B)



212-238V (SWITCH TO 'A')
224-251V (SWITCH TO 'B')



224-251V (SWITCH TO 'A')
235-265V (SWITCH TO 'B')



WQH8153

Line Voltage Selection Fig.5.1

POWER LEAD

5.4 Fit a suitable plug to the power lead in accordance with the standard colour code:-

	European	American
LINE	Brown	Black
NEUTRAL	Blue	White
EARTH (GROUND)	Green/Yellow	Green

AC POWER SUPPLIES CHECK

Resistance Check

5.5 With the power lead disconnected check the resistance of the transformer primary circuit (including FS50) using the multimeter (Table 3 item 1). The resistance should be as shown in Table 4.

TABLE 4

Power Supply Resistance Measurement

Voltage Selected	S52 Position	
	LO	HI
94-106/106-119	35Ω ± 6Ω	39Ω ± 7Ω
106-119/118-132	39Ω ± 7Ω	44Ω ± 7Ω
188-212/200-225	122Ω ± 18Ω	130Ω ± 20Ω
200-225/212-238	130Ω ± 20Ω	138Ω ± 20Ω
212-238/224-251	138Ω ± 20Ω	145Ω ± 22Ω
224-251/235-265	145Ω ± 22Ω	153Ω ± 22Ω

Supply Rail Voltages

5.6 (1) Remove the covers and prepare the power supply as described in the preceding paragraphs. Check that the a.c. supply voltage is correct.

(2) Set the power source selector on the rear panel to LINE POWER.

(3) With power supply connected, switch POWER to ON.

(4) Using the multimeter (Table 3 item 1) check the d.c. voltages at the following points on the main p.c.b. Fig.3 at the back of the book shows the component layout.

Test Point	Measurement	Remarks
TP3	+4.95 V ± 0.15 V	Relative to chassis or TP5
TP6	-4.9V ± 0.25V	
TP2	+24V ± 2.4V	

NOTE: There are no adjustments in the power supply circuit. If the 5V supplies are outside the limits given above, the supply voltage, the transformer primary connections and the setting of S52 should be carefully checked. If these are correct the zener reference diode D30 should be checked.

Ripple Level

5.7 Connect the variac (Table 3, item 9) to the local a.c. supply, and power the unit under test (UUT) from the variac. Monitor the variac output with the multimeter (Table 3, item 1), and adjust to give the minimum voltage of the range which suits the local supply.

5.8 Using the oscilloscope (Table 3, item 2) monitor TP4 and TP6 using a.c. coupling. The power supply 100Hz ripple should be less than 150mV peak to peak.

BATTERY POWER SUPPLIES CHECK

Charging Rate Checks

5.9 The charging rate can be checked only when the battery pack is fitted. It can be checked by inserting a multimeter, set to an appropriate current range, in series with the battery lead, or by measuring the volt drop across a charge path resistor and calculating the current. The latter method is recommended. Measurement is made with a.c. supplies connected and the POWER switch ON.

WARNING: LETHAL VOLTAGES ARE EXPOSED

5.10 For the A Battery, (+ 5 volts), voltage measurement should be made across the 3.9Ω resistor R128. This is accessible from the top of the main p.c.b.

5.11 For the B Battery, (- 5 volts), voltage measurement should be made across the 39Ω resistor R138. This measurement can also be made from the top of the main p.c.b.

5.12 Measurements should be made across both resistors with the rear panel switch in both the LINE POWER and CHARGE positions to allow calculation of the trickle charge and full charge rates respectively. The charging current varies considerably according to the state of charge. Nominal values during the middle of the charge period are:

		Current	Voltage across R128
Battery A	Trickle charge	85mA	0.33V
	Full charge	630mA	2.46V

		Current	Voltage across R138
Battery B	Trickle charge	6mA	0.23V
	Full charge	60mA	2.3V

Battery Economy Check

5.13 This check can be carried out without the battery pack fitted. Set the UUT controls as follows:

(1) Power source selector on the rear panel to LINE POWER

(2) OPERATE/STANDBY switch to STANDBY

(3) POWER switch to ON. After approximately a minute the display should blank out and the OVERFLOW/STANDBY indicator should light.

5.14 Press and release the RESET button. The display should indicate all zeros and the OVERFLOW/STANDBY indicator should be extinguished. After approximately one minute the display should again blank out and the OVERFLOW/STANDBY indicator should light.

PERFORMANCE TESTS AND CALIBRATION

NOTE: The procedures detailed in the following paragraphs may be carried out using line or battery supplies (provided the battery pack option is fitted). If battery supplies are to be used for performance testing it is desirable that the batteries be in the fully charged condition at the commencement of testing. No test result obtained when the Battery Low indicator is lit should be considered valid.

Segment, Decimal Point and Self Check

5.15 (1) Set the POWER switch to ON.

(2) Set the NORMAL/BURST/CHECK switch to CHECK.

(3) Select INPUT 'A'.

(4) Set the OPERATE/STANDBY switch to OPERATE.

5.16 Set the RESOLUTION switch as shown in Table 5 and verify that the correct displays are obtained.

TABLE 5

Segment and 'A' Channel Decimal Point Check

Resolution	Display
1 kHz	88888.888 MHz
100 Hz	8888.8888 MHz
10 Hz	888.88888 MHz
1 Hz	88888.888 kHz

5.17 Select INPUT 'B', and with the RESOLUTION switch set as shown in Table 6 verify that the correct displays are obtained.

TABLE 6

'B' Channel Decimal Point and Self Check

Resolution	Display
0,1 Hz	1000.0000 kHz
1 Hz	01.000000 MHz
10 Hz	001.00000 MHz
100 Hz	0001.0000 MHz

5.18 Set the input selector to LF and the NORMAL/BURST/CHECK switch to NORMAL. With the RESOLUTION switch set as shown in Table 7 verify that the correct displays are obtained.

TABLE 7

LF Decimal Point Check

Resolution Switch Setting	Display		
	With LF Option	Tolerance	Without LF Option
100 Hz	00000.000 kHz	+ 1 count	88888.888 kHz
10 Hz	0000000.0 Hz	+ 1 count	8888888.8 Hz
1 Hz	000000.00 Hz	+ 5 counts	888888.88 Hz
0.1 Hz	00000.000 Hz	+ 50 counts	88888.888 Hz

Sensitivity and Burst Check, Channel 'B'

5.19 Equipment required:

Item	Table 3 Item No.
Signal Generator	4
T piece	6
Terminating pad	7
Coaxial leads	8

5.20 Connect the T piece to the 'B' Channel input socket of the UUT. Connect the signal generator and the terminating pad to the T piece.

5.21 Set the controls of the UUT as follows:

(1) NORMAL/BURST/CHECK switch to NORMAL.

(2) OPERATE/STANDBY switch to OPERATE.

(3) Channel 'B' selected.

(4) RESOLUTION switch to 10 Hz.

5.22 Set the signal generator output to 62 MHz at a level of 10 mV r.m.s. Set R85 to the mid point of the range over which counting is stable. Apply the frequencies shown in Table 8 at a level of 8 mV r.m.s. (-29 dBm) with the RESOLUTION switch set as indicated. Verify that a stable and accurate display is obtained at this level.

NOTE: If it has been necessary to change IC30 measure the input level required to give stable counting with both C12 and R170 fitted. If the level is less than 4.5 mV r.m.s. remove C12. If the level is greater than 7.5 mV remove R170.

TABLE 8

'B' Channel Sensitivity

Frequency	Resolution	Display
10 Hz	0.1 Hz	0000.0100 kHz
1 kHz	1 Hz	00.001000 MHz
10 MHz	10 Hz	010.00000 MHz

5.23 Remove the T piece from the 'B' Channel input and select BURST. Press and release the RESET button, and verify that the numerals of the display go out but the decimal point remains.

5.24 Set the signal generator to an output of 62 MHz at a level of just greater than 20 mV r.m.s. (-21 dBm). Reconnect the T piece to the 'B' Channel input. Check that the display shows all zeros until the end of the gate period and then indicates the applied frequency.

5.25 Press and release the RESET button and check that the frequency displayed at the end of the gate period is correct. Set the NORMAL/BURST/CHECK switch to NORMAL and verify that the same frequency is indicated.

Sensitivity and Burst Check, Channel 'A'

5.26 Equipment required:

Item	Table 3, Item No.
Multimeter	1
Signal Generator	4
Coaxial leads	8

5.27 Connect the signal generator to the 'A' Channel input socket of the UUT.

5.28 Set the controls of the UUT as follows:

(1) NORMAL/BURST/CHECK switch to NORMAL.

(2) OPERATE/STANDBY switch to OPERATE.

(3) Channel 'A' selected.

(4) Resolution switch to 100 Hz.

5.29 Rotate R64 fully anticlockwise. Apply a signal of 530 MHz at a level of 7mV r.m.s. (-30 dBm) to the UUT and rotate R64 clockwise until the instrument counts correctly.

5.30 Apply the frequencies shown in Table 9 at a level of 8mV r.m.s. (-29 dBm) with the RESOLUTION switch set as indicated. Verify that a stable and accurate display is obtained at this level.

TABLE 9

'A' Channel Sensitivity

Frequency	Resolution	Display
400 MHz	1 kHz	00400.000 MHz
300 MHz	100 Hz	0300.0000 MHz
210 MHz	100 Hz	0210.0000 MHz
90 MHz	10 Hz	090.00000 MHz
38 MHz	10 Hz	038.00000 MHz

5.31 Press and release the RESET button. Verify that the display resets to zero.

5.32 Apply 38 MHz to the input and monitor the voltage at the AGC output pins on the rear panel. Check that the AGC voltage becomes more positive as the input level increases from zero to 100 mV r.m.s. (-7 dBm) and remains within the range 1± 0.2 volts 6 ± 1 volts.

5.33 Disconnect the signal from the 'A' Channel input and select BURST. Press and release the RESET button and verify that the numerals of the display go out but the decimal point remains.

5.34 Set the signal generator to an output of 520 MHz at a level of just greater than 20 mV r.m.s. (-21 dBm). Connect the signal generator to the 'A' Channel input. Check that the display shows all zeros until the end of the gate period and then indicates the applied frequency.

5.35 Press and release the RESET button and check that the frequency displayed at the end of the gate period is correct. Set the NORMAL/BURST/CHECK switch to NORMAL and verify that the same frequency is indicated.

5.36 Set the RESOLUTION switch to 1 Hz and check that the OVERFLOW indicator lights.

Overload Indicator Check

5.37 Equipment required:

Item	Table 3 Item No.
Signal Generator	4
Power Amplifier	5
Coaxial leads	8

5.38 Connect the signal generator to the power amplifier input. Connect the power amplifier output to the 'A' Channel input of the UUT.

5.39 Set the controls of the UUT as follows:

(1) NORMAL/BURST/CHECK switch to NORMAL

(2) OPERATE/STANDBY switch to OPERATE

(3) Channel 'A' selected

(4) RESOLUTION switch to 10 Hz

5.40 Set the output of the signal generator to a level which will give a power amplifier output of 8 volts r.m.s. at 60 MHz. Check that the OVERLOAD indicator on the UUT lights.

5.41 Reduce the input level to the power amplifier until the OVERLOAD indicator is extinguished. Check that the display shows the applied frequency.

Frequency Standard Check

5.42 Equipment required:

Item	Table 3 Item No.
Oscilloscope	2
Frequency Standard	3
T piece	6
Coaxial leads	8

5.43 Connect the oscilloscope to monitor the 1 MHz OUTPUT socket on the rear panel of the UUT. Connect a T piece to the frequency standard output and connect one end of the T piece to the oscilloscope external trigger input.

5.44 Set the oscilloscope to External Trigger and to a time base of 1 μs/cm.

5.45 Verify that the amplitude of the monitored signal is at least 3 volts peak to peak.

5.46 Connect the free end of the T piece to the UUT rear panel EXTERNAL STANDARD socket. Check that the trace observed on the oscilloscope locks, and that the EXTERNAL STANDARD indicator lights.

Internal Frequency Standard Calibration

.47 Equipment required:

Item	Table 3 Item No.
Oscilloscope	2
Frequency Standard	3
Coaxial leads	8

5.48 Connect the oscilloscope to monitor the 1 MHz OUTPUT socket on the rear panel of the UUT. Connect the frequency standard to the external trigger input of the oscilloscope. Set the oscilloscope to External Trigger.

5.49 When the frequency standard and the UUT have been switched on for at least one hour set the oscilloscope time base speed according to the internal frequency standard fitted. Adjust the internal frequency standard (if necessary) to ensure that the drift of the displayed waveform is less than 1 cm in 10 seconds.

TABLE 10

Internal Frequency Standard Calibration

Frequency Standard	Time Base Setting	Cycles of Waveform per cm
9442 (04A)	100ns/cm	0.1
9421 (04B)	100ns/cm	0.1
11-1254 (04C)	1 μs/cm	1

LF Multiplier

5.50 Equipment required:

Item	Table 3 Item No.
Signal Generator	4
T piece	6
Terminating pad	7
Coaxial leads	8

5.51 Connect the T piece to the 'B' Channel input of the UUT. Connect the signal generator and the terminating pad to the T piece.

5.52 Set the controls of the UUT as follows:

(1) NORMAL/BURST/CHECK switch to NORMAL

(2) OPERATE/STANDBY switch to OPERATE

(3) LF selected

(4) RESOLUTION switch to 1 Hz

5.53 Apply the frequencies shown in Table 11 at a level of 8 mV r.m.s. (-29 dBm). Verify that a stable and accurate display is obtained at this level. Increase input to 50 kHz and reduce again to 25 kHz. Observe multiplier does not lock to intermediate frequency.

TABLE 11

Frequency	Display
10 Hz	000010.00 Hz
25 kHz	025000.00 Hz

5.54 Remove the input connection to the UUT and check that the display does not exceed 5 counts.

DISMANTLING AND REASSEMBLY

Removal of Display PCB

5.55 (1) Disconnect the power supplies and remove the instrument covers (see paragraph 5.1).

(2) With a flat screwdriver prise off the cap on each carrying handle boss. Remove the screws now exposed and remove the handle.

(3) Slide back the short length of metal trim at each side of the instrument into the space normally occupied by the handle boss. This will expose the screws which secure the front panel.

(4) Remove the cap from the arm of the RESOLUTION switch.

(5) Unsolder the three earth braids on the underside, the coaxial connection from input A and the RESET switch connections.

(6) Unsolder the resistor and capacitor at input B from the pins on the display board.

(7) Remove the screws securing the front panel and withdraw the front panel and display p.c.b. as far as the wiring permits.

(8) Remove the seven screws securing the display p.c.b. to the front panel, allowing the p.c.b. and panel to be separated.

5.56 Reassembly is carried out in the reverse manner. Care must be taken not to damage the edge connector during reassembly.

Removal of Main PCB

5.57 With the top and bottom instrument covers removed all the main p.c.b. components are accessible for servicing, so the need for complete removal will be rare.

5.58 (1) Remove the upper and lower instrument covers as described in paragraph 5.1.

(2) Remove the caps from the arms of the RESOLUTION switch and the LINE POWER/CHARGE/BATTERY POWER switch.

(3) Remove the battery pack, if fitted.

(4) Unsolder the connections between the main p.c.b. and the rear panel components and completely remove the rear panel.

(5) Unsolder the connections to the LF multiplier, if fitted, and the connections to the three transistors on the left hand side panel.

(6) Unsolder the connections to the two smoothing capacitors and withdraw them until the lugs are clear of the holes in the p.c.b. Note the polarity of the connections.

(7) Unsolder the two wires between the main p.c.b. and the POWER switch.

(8) Unsolder the coaxial connection between input 'A' and the p.c.b.

(9) Unsolder R200 from the pin on the display p.c.b.

(10) Unsolder the three earth braids on the underside.

(11) Remove the four screws securing the main p.c.b. and slide it out to the rear.

5.59 Reassembly is carried out in the reverse manner. If it has been necessary to cut the tie for the smoothing capacitors replace it with Racal-Dana part number 24-0155.

FITTING FREQUENCY STANDARD 9421 or 9442

5.60 It should be noted that the frequency standard model 9421 cannot be fitted if the battery pack is fitted.

5.61 Remove the top cover of the instrument (see paragraph 5.1). Unsolder the three leads from the fitted frequency standard. Remove the retaining screws (and spacers in the case of the discrete component oscillator) and the black plate (if fitted). Remove the frequency standard.

5.62 Attach the replacement frequency standard to the inner face of the rear panel using the retaining screws removed in the previous paragraph.

5.63 Solder the leads from the main p.c.b. pins 30, 29 and 28 to the frequency standard base pins 1, 4 and 7 respectively. If model 9421 has been fitted ensure pins 5 and 6 on its base are linked.

5.64 Carry out the instrument check procedure to verify satisfactory functioning, and calibrate the frequency standard as detailed in paragraphs 5.47 to 5.49.

5.65 Replace the instrument cover.

FITTING BATTERY PACK 11-1289

5.66 The battery pack option consists of the following items:-

Item	Racal-Dana Part Number	Quantity
Battery Pack Assembly, complete with batteries and connecting lead.	11-1274	1
Mounting bracket	11-1239	1
Locating pegs	14-1486	2
Screws M4	24-7729	4
Washers, plain, M4	24-2705	2
Washers, crinkle, M4	24-2802	4

Fitting Procedure

5.67 (1) Disconnect the a.c. supply and remove the top cover (see paragraph 5.1).

(2) Screw the two locator pegs into the threaded holes in the inner face of the right hand side member, as seen from the front of the instrument.

(3) Place the mounting bracket against the inside of the left hand side member with the large hole over the carrying handle nut. Secure it to the side member with two M4 screws and crinkle washers.

(4) Take the battery pack, with the batteries uppermost and the connecting lead to the left, and carefully place the holes in the right hand end over the locator pegs. Lower the left hand end onto the bracket, and secure it with two M4 screws fitted with both plain and crinkle washers. The crinkle washers should be immediately below the screw heads.

(5) Plug the connecting lead onto pins 48 to 51 on the main p.c.b. just to the right of the power transformer. The pins are polarized to prevent incorrect connection.

(6) Replace the top cover. Set the rear panel switch to CHARGE, connect the instrument to suitable a.c. supplies and set the POWER switch to ON.

(7) When the batteries are fully charged check the operation of the instrument on battery power.

FITTING LF MULTIPLIER 11-1255

5.68 Before fitting the LF multiplier check that LK2 is fitted and LK1 is not fitted on the p.c.b. 19-0797.

5.69 (1) Remove the top cover (see paragraph 5.1). Remove the battery pack, if fitted.

(2) If model 9421 or model 9442 frequency standard is fitted detach it from the rear panel by removing the two retaining screws. It is not necessary to unsolder the connections.

(3) Attach the LF multiplier p.c.b. to the side panel using the screws, washers and spacers provided. Threaded mounting holes are provided in the right hand side towards the rear of the instrument.

(4) Connect pins 1 to 5 of the LF multiplier to the main p.c.b. in accordance with the circuit diagram (Fig.4). Dress the wiring neatly.

(5) Remove LK1 on main p.c.b. 19-0887.

(6) Refit the frequency standard to the rear panel.

(7) Carry out the instrument check procedure to verify satisfactory functioning. Replace the instrument cover.

SECTION 3

PARTS LISTS

CIRCUIT DIAGRAMS

AND

COMPONENT LAYOUTS

PARTS LIST

DISPLAY ASSEMBLY 19-0888

Note: Components are prefixed '1' on the circuit diagram.

Part No.	Description	Rat.	Tol %	Value	Component Reference
Resistors		W		Ω	
20-2331	Carbon Film	$\frac{1}{4}$	5	330	R1,2
20-2471	Carbon Film	$\frac{1}{4}$	5	470	R3
20-5500	DIL Array 7x56				R4
Integrated Circuit					
22-4128	BCD to 7 Segment Decoder (74247)				IC 1
Switches					
23-4099	Switch, Slide, 2 Position				S3
23-4100	Switch, Slide, 3 Position				S1,2
Indicators					
26-1508	Numerical Display, l.e.d.				DI 1 to DI 8
26-5004	Indicator, l.e.d.				LP 1 to LP 8
Capacitors		V		F	
21-1610	Ceramic	100	+80 -20	10n	C1,2,3,4, 5,6,7

PARTS LIST

5 MHz CRYSTAL OSCILLATOR ASSEMBLY (19-0834)

Part No.	Description	Rat	Tol %	Value	Component Reference
	Resistors	W		Ω	
20-2101	Carbon Film	¼	5	100	R1
20-2102	Carbon Film	¼	5	1k	R2
20-2103	Carbon Film	¼	5	10k	R4
20-2153	Carbon Film	¼	5	15k	R3
	Capacitors	V		F	
21-1616	Ceramic	12	20	100n	C1
21-2621	Silver Mica	125	5	27p	C5
21-2631	Silver Mica	125	5	330p	C2,3
21-6030	Trimmer			2-15p	C4
	Transistors				
22-6017	Silicon NPN (2N2369)				Q1
	Crystal				
17-2087	Crystal Assembly, 5 MHz				XL1

PARTS LIST

CHASSIS, FRONT AND REAR PANELS

Part No.	Description	Rat.	Tol %	Value	Component Reference
CHASSIS ASSEMBLY 11-1305					
20-3470	Resistor, Metal Oxide	½W	5	47Ω	R200
21-0575	Capacitor, Electrolytic	16V		4700μF	C101
21-0576	Capacitor, Electrolytic	25V		220μF	C102
22-6081	Transistor, npn (MJE 520)				Q51, 52
22-6139	Transistor, pnp (MJE 371)				Q50
FRONT PANEL ASSEMBLY 11-1310					
21-4528	Capacitor, Polyester	400V	10	47nF	C100
23-3030	Socket, BNC				SK50, 51
23-4013	Switch				S50
23-4097	Switch				S53
REAR PANEL ASSEMBLY 11-1311					
11-1254	Oscillator Assembly (refer to Parts List 2)				
17-4056	Transformer				T50
22-1650	Bridge Rectifier (VS248) 200V, 2A				D50
23-0031	Fuselink (94V to 132V) 250mA, surge resisting				FS50
23-0043	Fuselink (188V to 265V) 125mA, surge resisting				FS50
23-0044	Fuseholder for FS50				
23-3005	Socket, BNC				SK52, 53
23-3222 or 23-3253	Power Input Filter/Connector				
23-4091	Switch				S52
24-3515	Barb, Feedthrough				

PARTS LIST

MOTHERBOARD ASSEMBLY 19-0887

Part No.	Description	Rat	Tol %	Value	Component Reference
	Resistors	W		Ω	
-1514	Carbon Film	0.1	5	100	R170
20-1515	Carbon Film	0.1	5	180	R19, 74, 164
20-1519	Carbon Film	0.1	5	68	R86, 167
-1521	Carbon Film	0.1	5	1K	R4, 7, 121, 123, 144
-1516	Carbon Film	0.1	5	220	R55
20-1522	Carbon Film	0.1	5	12	R6, 8
20-1526	Carbon Film	0.1	5	22	R153
-1528	Carbon Film	0.1	5	2.2K	R5, 12, 24, 162, 169
-1529	Carbon Film	0.1	5	33	R72
20-1530	Carbon Film	0.1	5	390	R20
20-1531	Carbon Film	0.1	5	47	R18
-1532	Carbon Film	0.1	5	470	R17, 22, 54, 71, 147
20-1536	Carbon Film	0.1	5	560	R26, 27, 28
538	Carbon Film	0.1	5	10K	R16, 21, 35, 69, 98, 99, 122, 159,
20-1541	Carbon Film	0.1	5	1.8K	R11, 14, 53
20-1542	Carbon Film	0.1	5	4.7K	R73, 80, 146, 163
-1544	Carbon Film	0.1	5	1.2K	R23, 51, 70
20-1547	Carbon Film	0.1	5	2.7K	R124
20-1550	Carbon Film	0.1	5	8.2K	R13, 31
-1551	Carbon Film	0.1	5	100K	R15, 165
20-1555	Carbon Film	0.1	5	15K	R161, 168
20-1561	Carbon Film	0.1	5	1M	R2, 32
-1571	Carbon Film	0.1	5	12K	R9
-1572	Carbon Film	0.1	5	47K	R30
-2006	Carbon Film	¼	5	3.3	R154
20-2101	Carbon Film	¼	5	100	R61, 112, 125
20-2102	Carbon Film	¼	5	1K	R126, 151
-2103	Carbon Film	¼	5	10K	R58, 67, 68, 76, 78, 79, 81, 82, 89, 90, 92, 96, 101, 103, 104, 110, 114, 127, 130, 157
106	Carbon Film	¼	10	10M	R43,
2122	Carbon Film	½	5	1.2K	R41
-2124	Carbon Film	¼	5	120K	R48,
-2150	Carbon Film	¼	5	15	R84, 87, 88
20-2151	Carbon Film	¼	5	150	R10, 118, 158
20-2152	Carbon Film	¼	5	1.5K	R115
-2155	Carbon Film	¼	10	1.5M	R131
-2181	Carbon Film	½	5	180	R83, 105
-2182	Carbon Film	¼	5	1.8K	R36, 77, 145
20-2220	Carbon Film	¼	5	22	R62, 142
20-2221	Carbon Film	½	5	220	R34, 52, 75, 106, 120, 156
-2222	Carbon Film	¼	5	2.2K	R60, 63, 66, 111, 148
20-2223	Carbon Film	½	5	22K	R59, 65, 113, 171
20-2271	Carbon Film	¼	5	270	R45
-2331	Carbon Film	¼	5	330	R44, 47, 119, 141
20-2332	Carbon Film	¼	5	3.3k	R136
20-2390	Carbon Film	¼	5	39	R50
-2391	Carbon Film	¼	5	390	R134
-2471	Carbon Film	¼	5	470	R57, 93
20-2472	Carbon Film	¼	5	4.7k	R33, 97, 117, 135
20-2473	Carbon Film	¼	5	47k	R155
-2822	Carbon Film	¼	5	8.2k	R102
-2475	Carbon Film	¼	5	4.7M	R49
-2561	Carbon Film	¼	5	560	R25, 132
20-2121	Carbon Film	¼	5	120	R56

Part No.	Description	Rat	Tol %	Value	Component Reference
	Resistors (Contd)				
20-2154	Carbon Film	¼	5	150K	R40
20-2225	Carbon Film	¼	10	2.2M	R39
20-2562	Carbon Film	¼	5	5.6K	R46, 91, 109, 129, 152, 160
20-2680	Carbon Film	¼	5	68	R37
20-2681	Carbon Film	¼	5	680	R29, 150
20-2682	Carbon Film	¼	5	6.8K	R100, 137
20-2820	Carbon Film	¼	5	82	R116
20-3103	Metal Oxide	½	5	10K	R38
20-3270	Metal Oxide	½	5	27	R133
20-3390	Metal Oxide	½	5	39	R42, 138
20-3470	Metal Oxide	½	5	47	R149
20-4094	Metal Oxide	¼	1	6.8K	R140
20-4103	Metal Oxide	¼	1	1.2K	R143
20-4107	Metal Oxide	¼	1	5.6K	R139
20-4658	Metal Oxide	1	5	100K	R3
20-5055	Wirewound	2½	5	3.9	R128
20-5501	DIL Array	8 x 220			R107
20-5502	DIL Array	13 x 1K			R108
20-5503	DIL Array	13 x 10K			R94, 95
20-7025	Variable			200	R85
20-7034	Variable			2K	R64
20-3680	Metal Oxide	½	5	68	R166
	Capacitors	V		F	
21-1002	Tantalum	20	20	10μ	C11, 68
21-1003	Tantalum	20	20	15μ	C13
21-1006	Tantalum	20	20	4.7μ	C30
21-1029	Tantalum	35	20	1.5μ	C31
21-1038	Tantalum	6.3	20	47μ	C4, 8, 10, 15, 18, 19, 23, 25, 26, 32, 39, 56, 59, 73, 75, 40, 82, 83, 84, 85, 86, 87, 88
21-1046	Tantalum	3	20	220μ	C7
21-1519	Ceramic	500	10	82p	C33
21-1513	Ceramic	500	10	27p	C22
21-1515	Ceramic	500	10	39p	C80
21-1516	Ceramic	500	10	47p	C1, 12
21-1518	Ceramic	500	10	68p	C28
21-1520	Ceramic	500	10	100p	C60
21-1528	Ceramic	500	10	470p	C65
21-1532	Ceramic	500	20	1n	C62, 79, 81, 90
21-1547	Ceramic	25	+50 -20	33n	C34
21-1548	Ceramic	12	+80 -20	47n	C16
21-1589	Ceramic	12	+80 -20	220n	C64, 69
21-1610	Ceramic	100	+80 -20	10n	C38, 41, 42, 43, 44, 45, 47, 50, 51, 52, 53, 55, 57, 58, 93
21-1616	Ceramic	12	+80 -20	100n	C2, 3, 6, 9, 14, 20, 21, 24, 27, 29 46, 54, 61, 63, 66, 67, 70, 71, 72, 74, 76, 77, 78, 89, 91, 92, 94, 96, 97, 98
21-1671	Ceramic	63	¼p	1.8p	C35
21-1680	Ceramic	63	¼p	10p	C48

PARTS LIST

MOTHERBOARD ASSEMBLY 19-0887

Part No.	Description	Rat	Tol %	Value	Component Reference
	Capacitors	V		F	
21-1686	Ceramic	63	2	33p	C49
21-1728	Ceramic	100	10	220p	C36
21-1504	Ceramic	500	½p	4.7p	C37
21-1503	Ceramic	500	½p	3.9p	C95
	Integrated Circuits				
22-4092	Schottky Dual 4-Input NAND Gate (74S20)				IC8
22-4111	High Performance Operational Amplifier (741)				IC29
22-4124	Schottky Triple 3-Input NAND Gate (74S10)				IC9
22-4202	Dual Frequency Compensated Operational Amplifier (747)				IC6,11,25,31
22-4204	Wideband UHF Amplifier (OM335)				IC26
22-4245	Differential Video Amplifier (Selected 72733)				IC30
22-4500	Decade Counter, 600MHz (SP8630B)				IC18
22-4528	Triple Line Receiver (MC10116P)				IC21
22-4530	Schottky Quad 2 to 1 Line Multiplexer (74LS157)				IC20,27
22-4531	Schottky Quad 2-Input NAND Gate (74LS00N)				IC5,15
22-4532	Schottky Quad 2-Input NOR Gate (74LS02N)				IC22
22-4533	Schottky Hex Inverter (74LS04N)				IC1,3,7,10
22-4534	Schottky Dual D Type Bistable (74LS74)				IC14,
22-4536	Schottky Decade Counter (74LS90)				IC23
22-4546	Schottky Quad 2-Input NAND Gate (74LS03N)				IC13,19,24
22-4552	Schottky 4 bit Full Adder (74LS283N)				IC16
22-4556	Schottky BCD to Decimal Decoder (74LS145N)				IC28
22-4557	Schottky Triple 3-Input NAND Gate (74LS10)				IC17
22-4601	CDI LSI (Racal-Dana)				IC4
22-4581	Dual Retriggerable Monostable (74LS221)				IC2
22-4516	Schottky Dual D Type Bistable (74S74)				IC12
	Diodes				
22-0007	Germanium (AAZ15)				D22
22-1029	Silicon (IN4149)				D1,2,3,6,7, 8,19,20,21,23, 24,25,27,29,35
22-1033	Silicon, Hot Carrier (HP5082.2811)				D4,5,16,17,18, 36
22-1058	Silicon, PIN (HP5082.3379)				D11,12,13,14,15
22-1068	Silicon, Hot Carrier (HP5082.2800)				D9,10
22-1807	Voltage Regulator (BZY88C4V7)				D28
22-1857	Voltage Regulator (BZX79C5V1)				D30

Part No.	Description	Rat	Tol %	Value	Component Reference
	Transistors				
22-6009	Silicon, npn (2N4124)				Q10,27,36
22-6010	Silicon, pnp (2N4126) 2N39..				Q3,37
22-6017	Silicon, npn (2N2369) or				Q2,8,15,16, 17,28,29,30, 31,35
22-6079					
22-6057	Silicon npn (ZTX342)				Q26
22-6079	Silicon, npn (ZTX313L)				Q5,11,12
22-6101	FET, N Channel (E300A)				Q1
22-6110	Silicon, pnp (BFX48)				Q4
22-6112	Silicon, npn (ZTX450)				Q7
22-6113	Silicon, pnp (ZTX550)				Q6,13,14,18, 19,20,21,22, 23,24,25,32, 33,34
22-6123	Silicon, npn (BFR90)				Q9
	Inductors				
17-3207	Inductor (to Racal-Dana Drawing)				L10
17-3208	Inductor (to Racal-Dana Drawing)				L6
23-7007	Choke RF sub-miniature			0.68µ	L8,11
23-7011	Choke RF sub miniature			3.3µ	L7
23-7014	Choke RF sub miniature			10µ	L3,5,9
23-7018	Choke RF sub miniature			47µ	L1,2
	Miscellaneous				
17-0084	Switch				S2
17-0085	Switch				S1
17-3214	Transformer				T1
23-0006	Fuse				FS1
23-0034	Fuse Holder for FS1				
23-3213	I.C. Holder for IC4				
23-7516	Relay RS 817-117				RLA
23-8029	Ferrite Bead				FX1

23-5150 Edge Connector main ... / display ...

16-0463 Corner moulding

11-1147 Handle

23-4097 Switch, Mains SS1

24-7024 rubber cover (inner) for rear case screw (Grommet)

23-9020 AERIAL
order from Panorama Antennas

24-0149 Switch (Power Selector & Resolution) Knob

15-9057 Handle cap

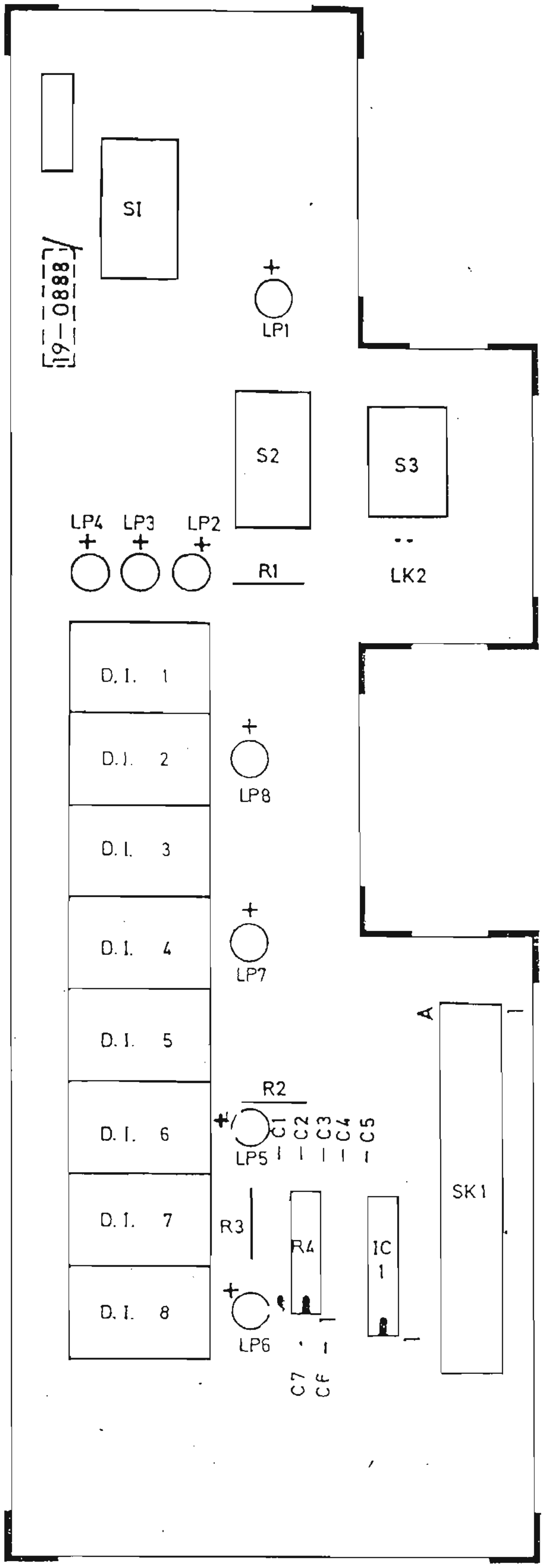
STC 73407A Mains LEAD

PARTS LIST : OPTION 09

LF MULTIPLIER ASSEMBLY 19-0797 FIG.6

NOTE: When fitting a new p.c.b. check that link LK2 is fitted, and not LK1.

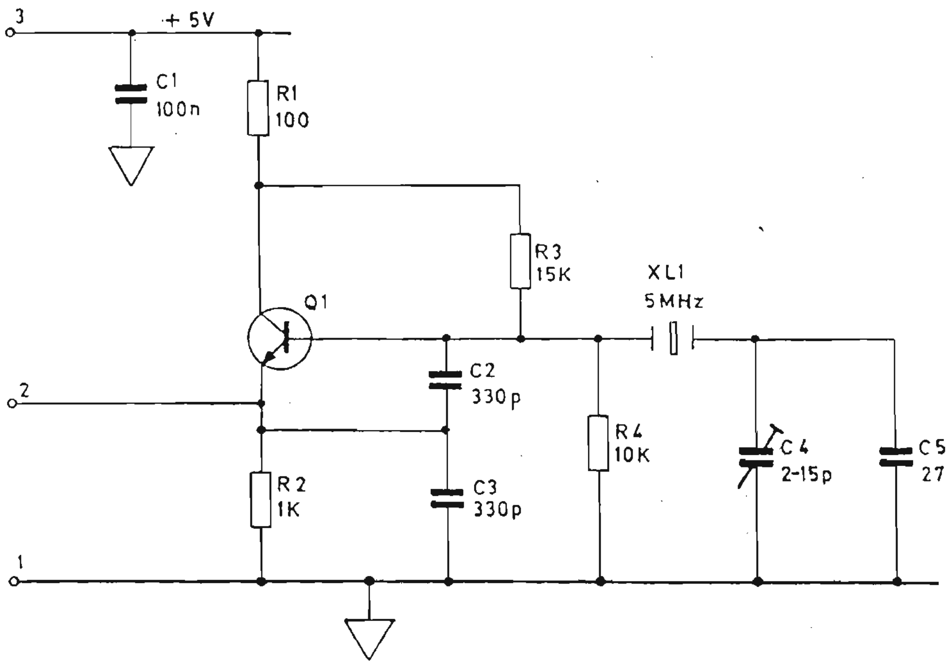
Part Number	Description	Rat	Tol. %	Value	Component Reference
	Resistors	W		Ω	
20-2101	Carbon Film	¼	5	100	R7
20-2102	Carbon Film	¼	5	1k	R9,11,12
20-2103	Carbon Film	¼	5	10k	R10
20-2105	Carbon Film	¼	5	1M	R4
20-2153	Carbon Film	¼	5	15k	R2
20-2392	Carbon Film	¼	5	3.9k	R8
20-2473	Carbon Film	¼	5	47k	R1,5
20-2562	Carbon Film	¼	5	5.6k	R6,
20-2564	Carbon Film	¼	5	560k	R3
	Capacitors	V		F	
21-1002	Tantalum	20	20	10μ	C5,6
21-1029	Tantalum	35	20	1.5μ	C1,2
21-1038	Tantalum	6.3	20	47μ	C3
21-1508	Ceramic	500	10	10p	C4,8
21-1532	Ceramic	500	20	1n	C7
	Diodes				
22-1029	Silicon(1N4149)				D1,2,3
	Integrated Circuits				
22-4121	Op.Amp. 8 pin d.i.l. (301)				IC1
22-4703	CMOS, Phase Lock Loop (4046)				IC2
22-4569	Dual Decade Counter				IC3
	Transistors				
22-6113	Silicon PNP (ZTX 550)				Q2
22-6017	Silicon NPN (2N2369)				Q3

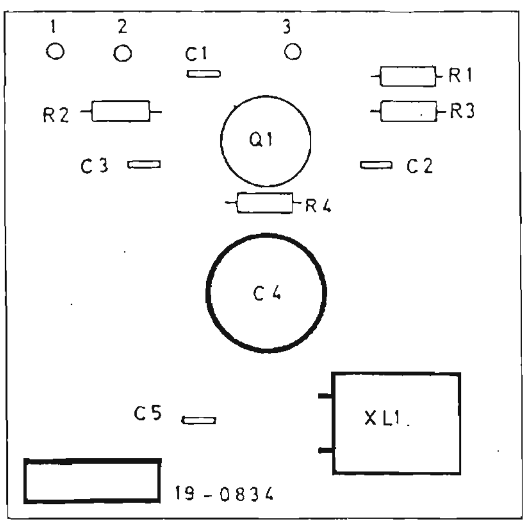


Component Layout:
Display Assembly 19-0888

RACAL
WOH 8153 19-0888
1 2

Fig. 1

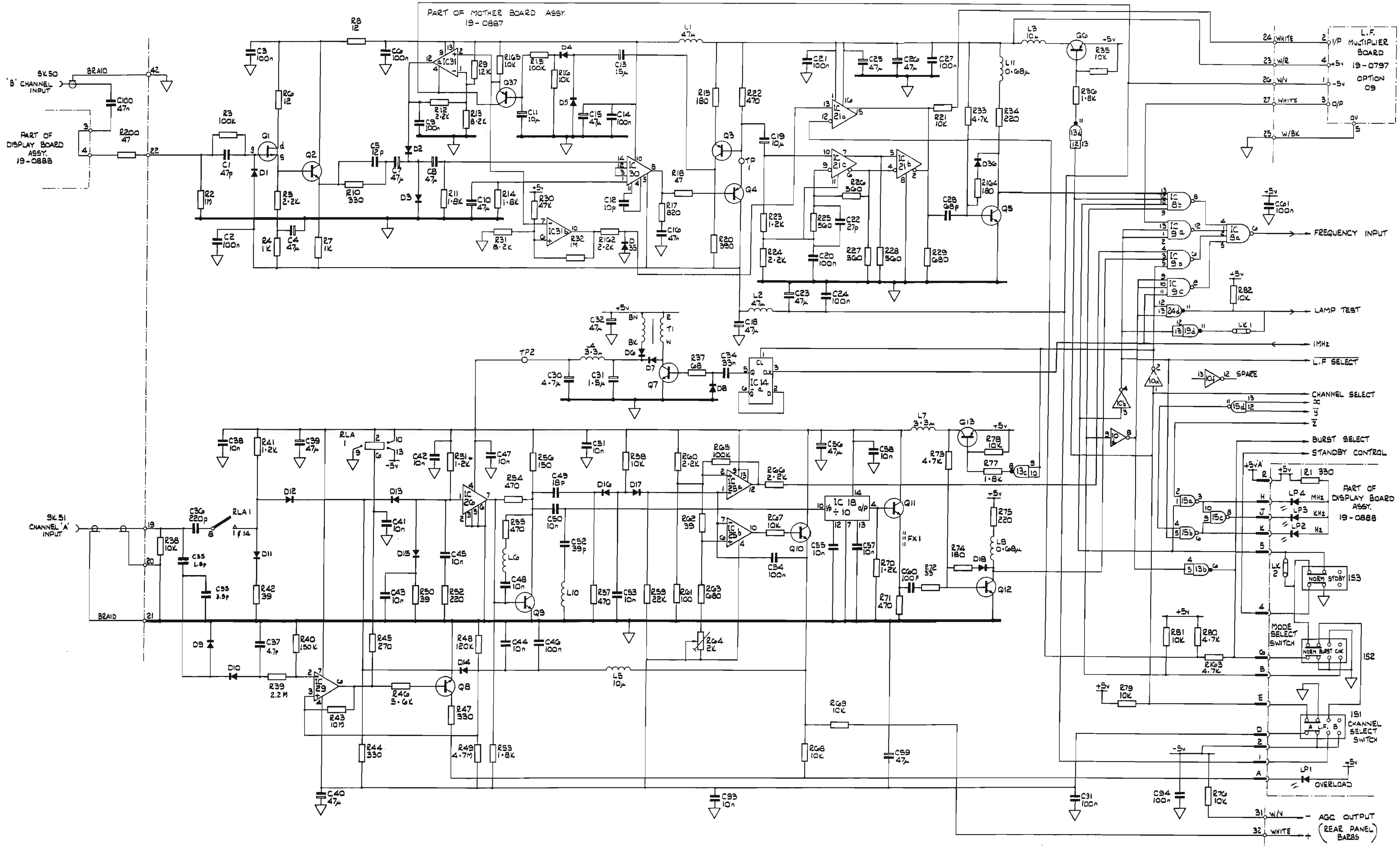




WOH	19-0834
1	

Circuit And Layout
5MHz Oscillator PCB 19-0834

Fig. 2



Overall Circuit Diagram,

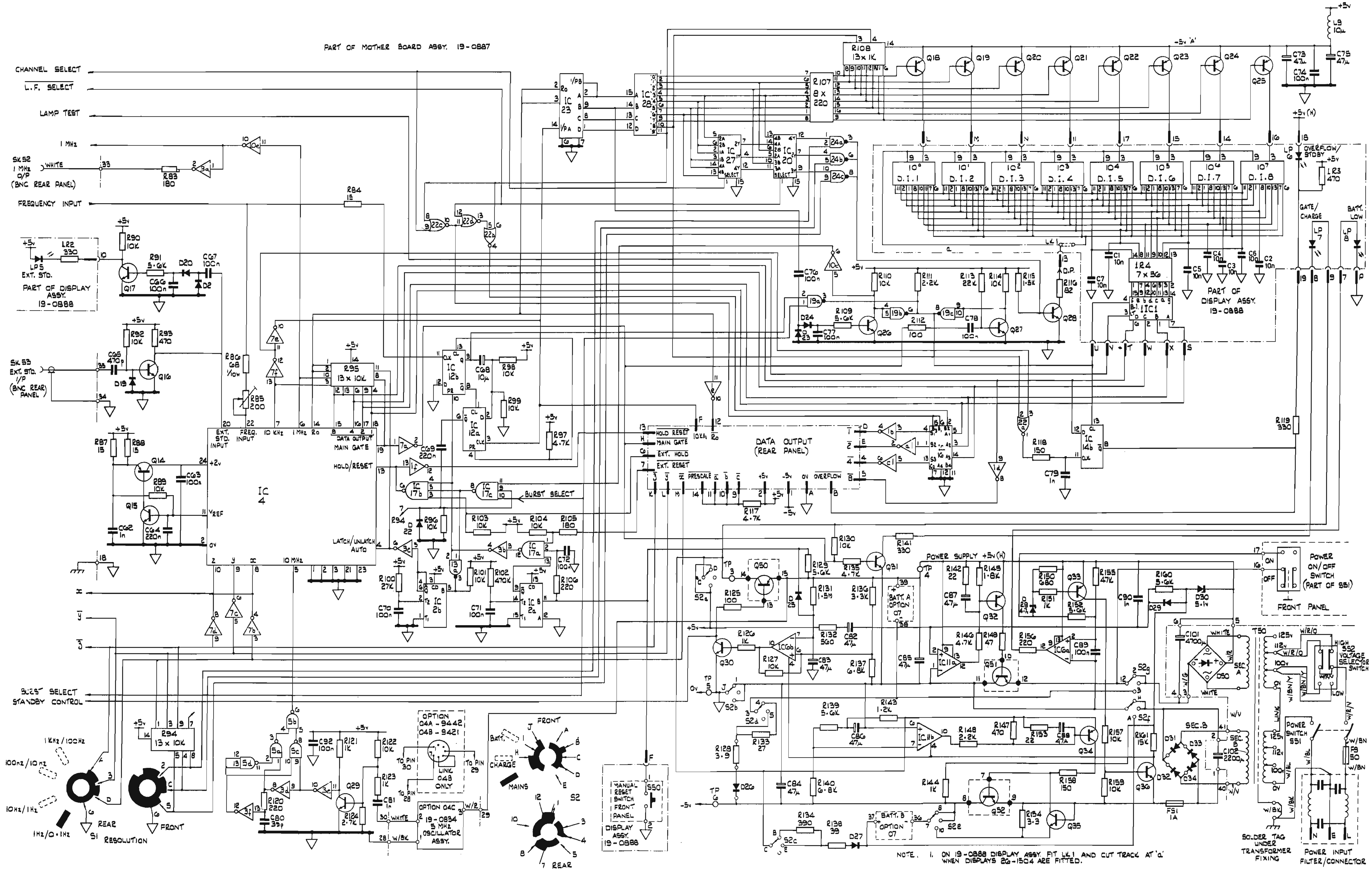
Part 1: 9916

Fig.4

RACAL

W0H8153

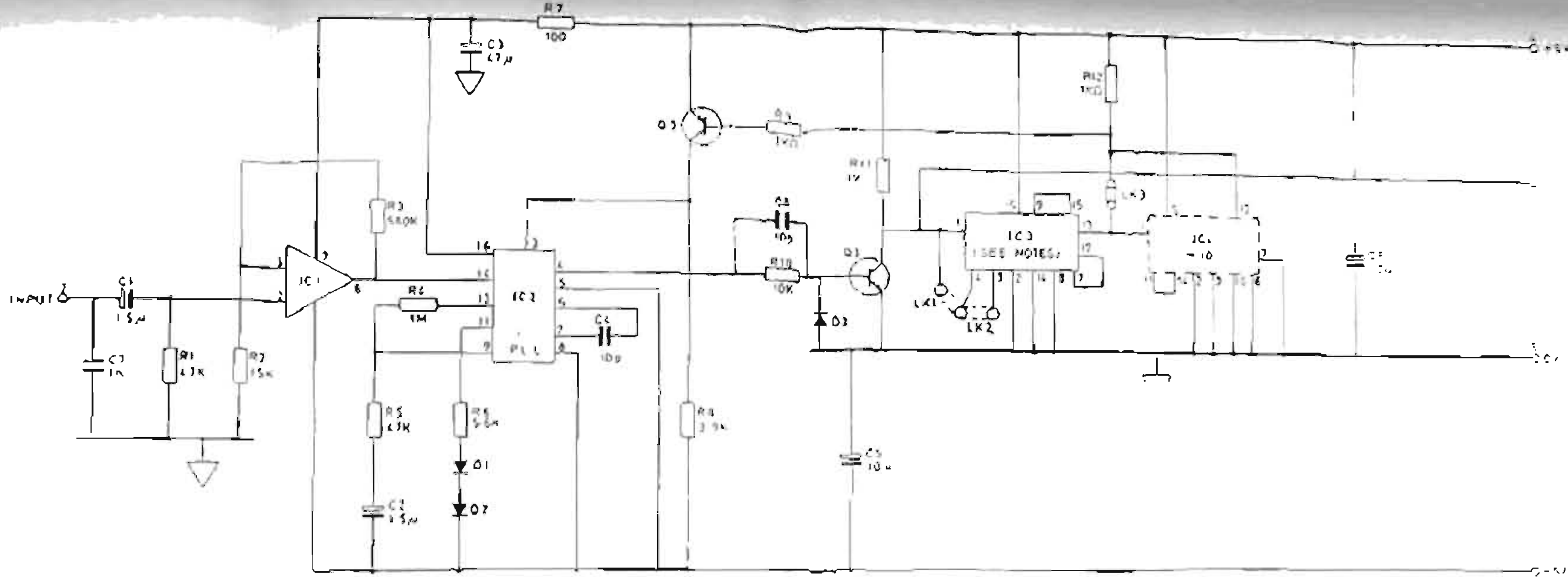
1

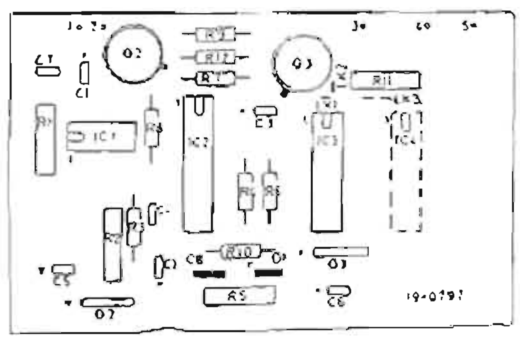


RACAL
WOH 8153
1 2

Overall Circuit Diagram,
Part 2: 9916

Fig.5





NOTES
1. LK1 FITTED ON [illegible]
2. LK2 FITTED ON [illegible]
3. LK3 FITTED ON ALL ABOVE MODELS
4. IC4 NOT NORMALLY FITTED

Circuit and Layout:
LF Multiplier Assembly

Fig 6

SECTION 4

APPENDICIES

AND

CHANGE INFORMATION

OPTION 01

SERIAL TO PARALLEL INTERFACE UNIT

CONTENTS

TABLES

SERIAL TO PARALLEL INTERFACE UNIT

OPTION 01

INTRODUCTION

1. The interface comprises a metal box, measuring approximately 132 x 95 x 36mm containing the p.c.b assembly 19-0851. Connections are made to printer or data display via a 50-way fixed socket and to the '99' instrument via a flying lead fitted with a 28-way edge connector. The unit is designed to operate with the following Racal counters, referred to in this description as the '99' series'

Frequency Meters		Universal Counter Timers (UCT)	
9910	9911	9900	9901
9912	9913	9902	9903
9914	9915	9904	9905
9916	9917	9906	
9917A	9919	9908	

2. Definition of Terms

(1) Hold Signal : a signal returned by the users equipment to the interface for control purposes.

(2) Print Command : a signal output by the interface to indicate that new measurement information is available.

(3) Print Hold input : An input which allows the user's Hold Signal to prevent the parallel information from changing.

(4) Hold/Reset input : An input which allows the user's signal to prevent the parallel information from changing and which resets the instrument when the Hold Signal returns to its normal state, thus starting a new measurement.

(5) Hold Control : An input to the interface which determines the mode of operation.

FUNCTION

3. The function of the Interface Unit is to convert the serial b.c.d. data output from a '99 series' counter to a static parallel form, suitable for driving a printer, data display or processing equipment.

4. The parallel output data is updated at the end of each gate time unless the printer (or other data processing equipment) is applying a Hold Signal. In addition to measurement data the interface also transfers information on decimal point position, selected range (gate time) and the 'overflow' state of the counter display. Information supplied is for 8 digits (excluding decimal point data) on all units except the 9917 and 1197A which supply information for 9 digits.

5. Fig. A1. shows the sequence of events which occurs at the end of the gate time. Note that when using counters 9910, 9911, 9912 and 9919, and when using counter 9908 on 'A' channel with AC coupling, all timings are doubled, except the print command pulse width.

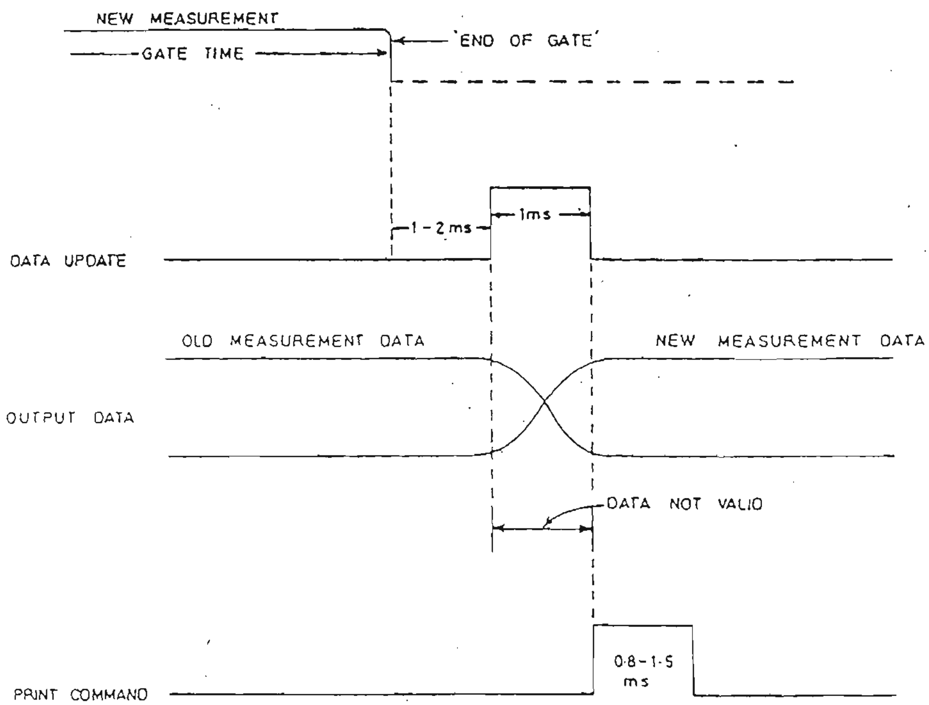


Fig. A1

CONNECTION

6. Before connecting the Interface Unit to the counter refer to the modes of operation in paras 8 to 18 and make the necessary changes to the 50-way connection or 28-way flying lead, according to the type of counter in use and the required function. All changes on the 50-way connection should be made at the customers connector.

7. Having checked the appropriate connection changes in paras 8 to 18, the interface should be connected up as follows:-

(1) Remove the black plate which covers the DATA OUTPUT aperture on the rear panel of the counter. Retain the two screws.

(2) Slacken off the cable clamp on the metal cover on the cable of the flying lead, and push the cover away from the connector.

(3) Plug the flying lead connector into the Data Output edge connector in the counter, noting the keyway which ensures correct orientation.

(4) To minimise r.f. radiation interference, the metal cover on the cables
(4) should be placed over the edge connector and held into place by the two screws which originally secured the cover plate removed in (1). The cable clamp should then be tightened.

(5) Connect the interface unit to the data processing equipment via the fixed 50-way socket.

MODES OF OPERATION

REMOTE DISPLAYS

Connections

8. If the interface is required to drive a remote display, or such other equipment that does not require the data to be held for a period longer than the gate time, check the following pin conditions on the 50-way connector:-

Pin No.	Required Connection
19	Must be either open circuit
24	or connected to OV.
49	

Latched Operation

9. The display is latched and is updated at the end of each gate time, irrespective of the counter function.

Unlatched Operation

10. (1) If the interface Unit is connected to a genuine remote display the subjective result is that the display will appear to follow the counter, for both latched and unlatched counter modes.

(2) The data outputs will be updated every 3 to 4 ms.

(3) The blue wire 'H' on the 28-way flying lead connector should be disconnected and reconnected to 'F' together with the violet wire. For other applications refer to paras 16 to 18.

USING EQUIPMENT WHICH PROVIDES HOLD SIGNALS

11. Differing instructions apply, depending on whether the counter is a frequency meter or universal counter timer (UCT) as described in paras 12 to 15.

Frequency Meters - Normal Use

12. (1) Check the following pin connections on the 50 way connector:-

Pin No.	Required Connection
19 and 24	Open Circuit, or connected to OV
49	Connected to the Hold signal

(2) The Hold signal (logic level '1' to hold) should be applied to the interface after receiving the Print Command signal, but before the end of the next gate time (ie 7 ms for 10 ms gate time), and should remain at logic level '1' for the period that the information on the data output is required to remain unchanged. Although the outputs from the interface will remain unchanged whilst a Hold is applied, the counter continues its normal measurement sequence, i.e. 'free run'. This has the advantage that the next Print Command will be given at the end of the gate time immediately following the release of the Print Hold. This result in a more rapid measurement sequence. From Fig. A2. it can be seen at a Print Command signal occurs 3 to 4 ms after an end of gate, by which time the gate time for a new measurement will have commenced.

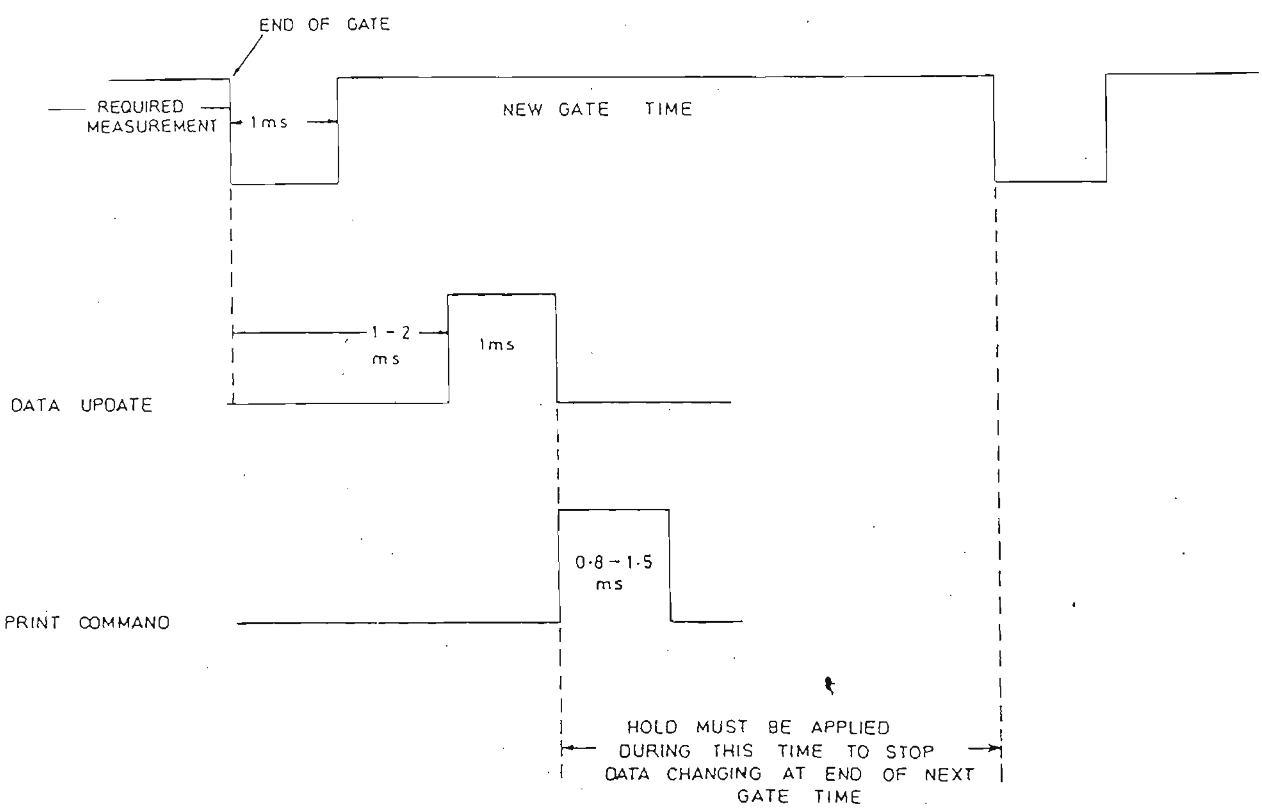


Fig. A2

13. The measurement cycle of the 99 series of UCT's has two distinct phases; the Gate Time during which the measurement is made, and the Display Time during which the results are displayed. If the hold time required by the equipment to which the interface is connected is less than the display time, the remainder of the display time is effectively wasted. The interface can be used to shorten the display time, but in so doing the counter display is reset, which may not be convenient. For this reason the interface can be used with UCT's in two modes, the Print Hold and the Hold/Reset modes, as described in paras 14 and 15. It should be noted that, with UCT's, the interface will not produce a data change or Print Command signal from the operation of a front panel RESET control.

UCT's Using Print Hold Mode

14. In the Hold/Reset mode the Hold signal extends the display time indefinitely the next gate time commencing when the Hold is released or when the normal display period has ended, whichever period is the longer. The Hold signal must be applied within the display time period in order to halt the measurement cycle. The required pin connections on the 50 way connector are as follows:-

Pin No.	Required Connection
Pin 19	Connected to Pin 50 (or to 5V via 180Ω)
Pin 49	Connected to the Hold signal source
Pin 24	To be open circuit or connected to OV

UCT's Using Hold/Reset Mode

15. In the Hold/Reset mode the Hold signal (minimum width 5 ms) extends the display time indefinitely, but when it is released the counter display resets and a new measurement commences. This result in a more rapid measurement sequence, again the Hold signal must be applied within the display time period in order to halt the measurement cycle. The required pin connections on the 50-way connector are as follows:-

Pin No.	Required Connection
Pin 19	Connected to pin 50 (or to 5V via 180Ω)
Pin 24	Connected to the Hold signal source
Pin 49	To be open circuit or connected to OV

SPECIAL APPLICATIONS

Remote Display-Special Applications

16. When used in the unlatched mode with certain types of equipment other than remote displays (for example a digital comparator) there is a limit to the maximum possible counting rate. Therefore the reading for which the comparator is looking could be missed, i.e. there is a maximum update rate for the option of 3-4 ms. This corresponds to an input frequency of 200 Hz (N=1) on Totalize mode and a maximum resolution of 10ms on Time Interval mode. The counting rate can be increased if a degree of overshoot can be tolerated.

The maximum overshoot that will occur is given by:-

$$\text{Counting Rate} \times 4 \times 10^{-3} \text{ counts.}$$

It is advisable to use the Print Command as a 'data valid' signal in such systems.

Frequency Meters - Special Applications

17. In some applications it is not possible to use the interface in the manner described in Para 12. For example, in control systems, where the output of the interface is used as feedback to the device on the input of the counter, problems arise because the next gate time has already started before the information becomes available from the previous one. Therefore, even if the feedback correction is made almost instantly, the reading at the end of the next gate time will be incorrect. Alternatively, if the correction process takes more than one gate time, the end of gate time immediately following the process will also give incorrect results. These problems may be overcome by applying a Hold signal to the Print Hold input (pin 49) for the length of time that the correction takes, plus an additional time to ensure that the gate time from which the next data is to be taken cannot start until the correction process has been completed, as shown in Fig. A3.

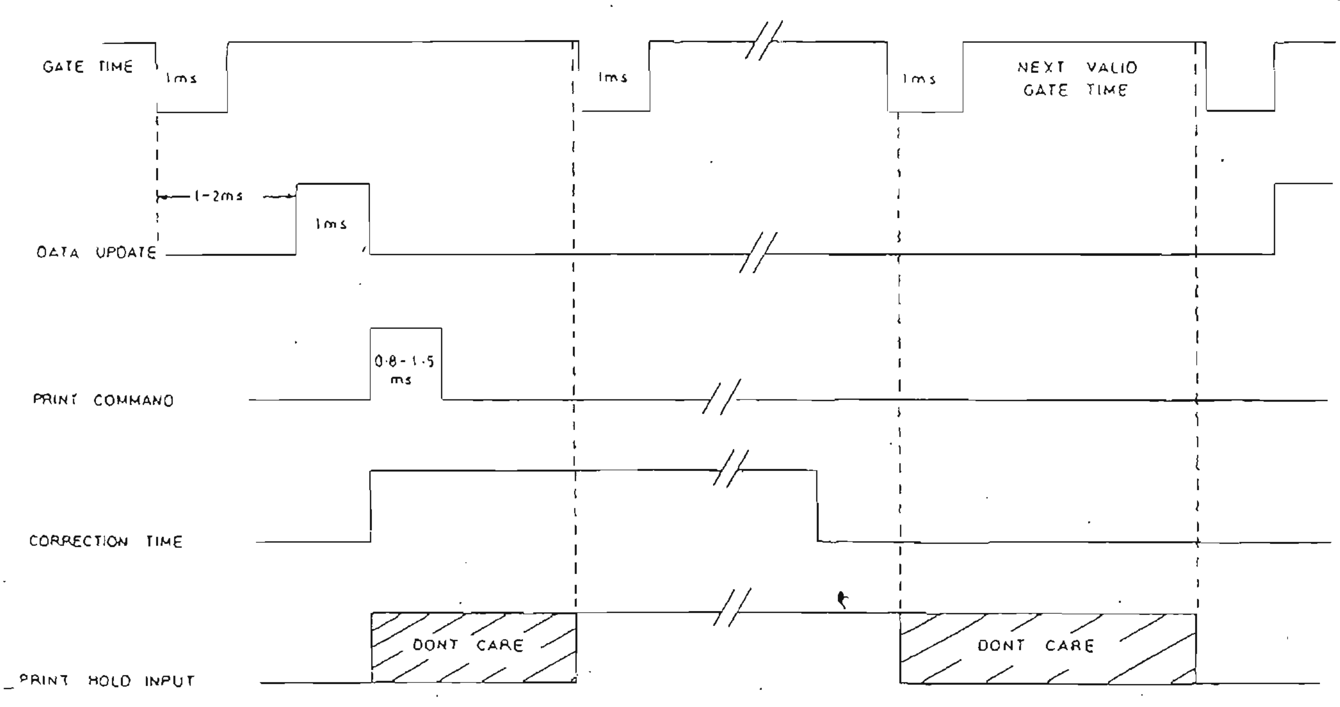


Fig. A3

18. An alternative to para 17, particularly when fast cycle times are desired, is to connect the Hold signal to the Hold/Reset input. If this is done, a stretched version must additionally be applied to the print Hold input (pin 49). The Hold signal should be at least as long as the correction process, and the signal applied to the Print Hold input should be approximately 200μs longer than that applied to the Hold/Reset input. This is to prevent the interface responding to the end of gate time produced by the reset. For cases where the correction time is short (less than the Print Command pulse width) this may be implemented by linking the Print Command output (pin 48) to the Hold/Reset input (pin 24) and by applying a stretched version of the Print Command to the Print Command to the Print Hold input (pin 49). In this way cycle times as short as 'Gate Time + 5ms' can be achieved. This is illustrated in Fig. A4.

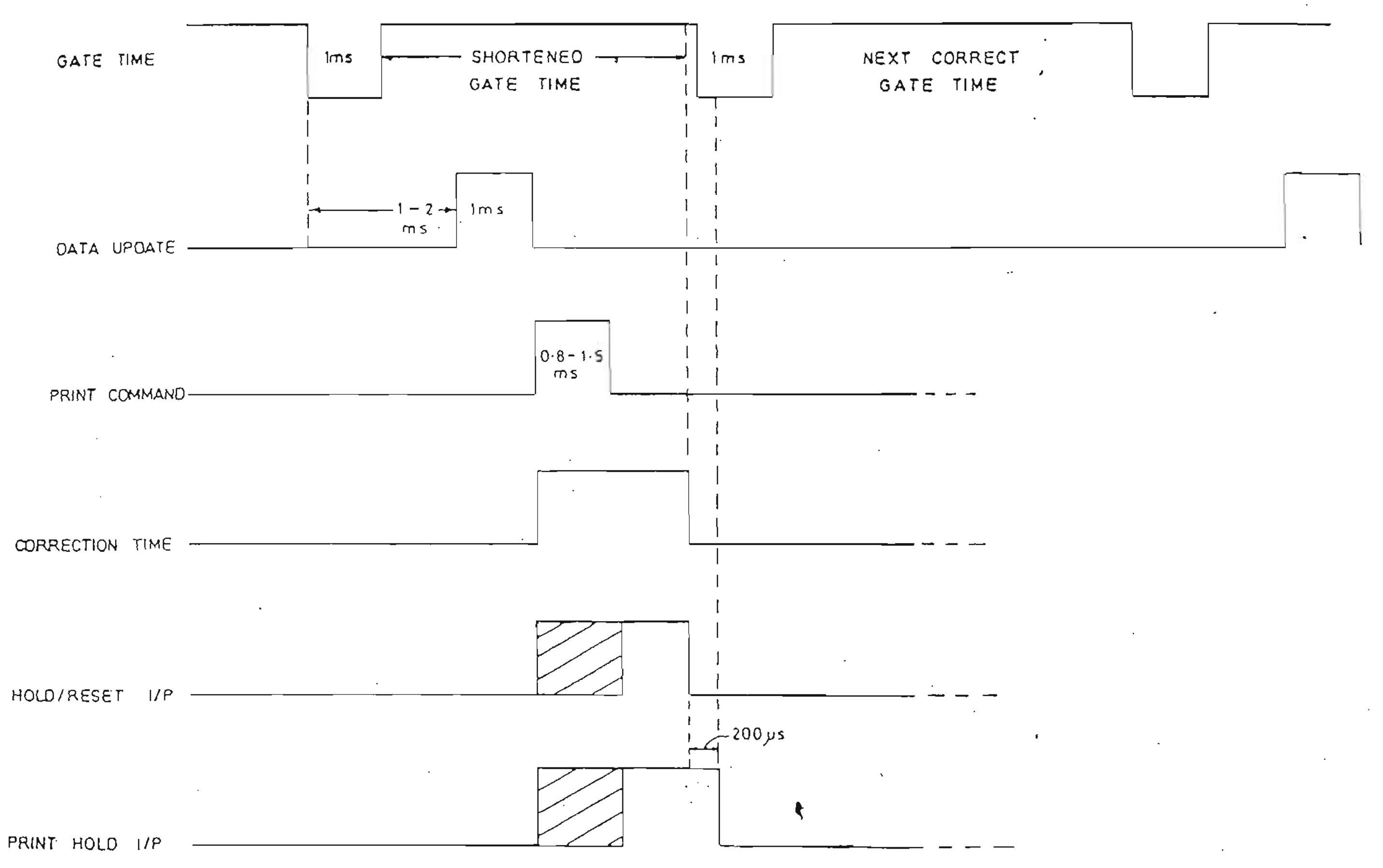


Fig. A4

TABLE 1.

FLYING LEAD CONNECTIONS

Pin No.		Pin No.	
1.	Not Connected	A	0V
2.	+ 5V (nominal)	B	$\overline{\text{OVERFLOW}}$
3.	KEYWAY	C	KEYWAY
4.	$\overline{4}$ BCD DATA	D	$\overline{1}$ BCD DATA
5.	$\overline{8}$	E	2
6.	$\overline{\text{COUNTER HOLD}}$	F	Multiplex Sync (Note 2)
7.	$\overline{\text{COUNTER RESET}}$	H	$\overline{\text{MAIN GATE}}$
8.	DIGIT 10^8 SELECT	J	Not Connected
9.	Not Connected	K	$\overline{Z}$)
10.	Not Connected	L	$\overline{Y}$) TIME BASE
11.	Not Connected	M	$\overline{X}$)
12.	$\overline{\text{Ro}}$	N	Not Connected
13.	$\overline{\text{HOLD/RESET}}$	P	Not Connected
14.	See NOTE 1	R	Not Connected

NOTE 1. In option 01 units with serial numbers after 1389, pin 14 of the flying lead connection is connected within the interface unit to pin 43 of the 50 way connector. This permits a remote indication when instruments are in the divide by ten prescale mode.

NOTE 2. The multiplex sync. signal on pin F is 10 KHz, except with 9911 and 9919 instruments when it is 5 KHz.

TABLE 2.

50-WAY CONNECTOR

Pin No.	Facility		Pin No.	Facility	
1.	1	10^0 DIGIT	26.	1	10^1 DIGIT
2.	2		27.	2	
3.	4.		28.	4	
4.	8		29.	8	
5.	1	10^2 DIGIT	30.	1	10^3 DIGIT
6.	2		31.	2	
7.	4		32.	4	
8.	8		33.	8	
9.	1	10^4 DIGIT	34.	1	10^5 DIGIT
10.	2		35.	2	
11.	4		36.	4	
12.	8		37.	8	
13.	1	10^6 DIGIT	38.	1	10^7 DIGIT
14.	2		39.	2	
15.	4		40.	4	
16.	8		41.	8	
17.	OVERFLOW		42.	4	10^8 DIGIT
18.	1	10^8 DIGIT	43.	See table 1 NOTE 1.	
19.	HOLD CONTROL I/P		44.	8	10^8 DIGIT
20.	2	10^8 DIGIT	45.	1	DECIMAL POINT
21.	$\overline{X}$	TIME BASE	46.	2	
22.	$\overline{Y}$		47.	4	
23.	$\overline{Z}$		48.	PRINT COMMAND O/P	
24.	HOLD/RESET I/P		49.	PRINT HOLD I/P	
25.	0V		50.	+ 5V (VIA 180Ω)	